

Block Diagram

NVHS

DP_F

DP_E

DP_D

DP/HDMI_C

MEM D

MEM C

MEM E

MEM F

NVHS x16

GA102
(GB5-384)

MEM B

MEM A

PCIe 4.0 x16 EDGE FINGER

NVVDD

Power Supply

NVVDD: PH1-10 OVR4+

MSVDD

Power Supply

MSVDD: PH1-6 OVR4+

FBVDDQ

Power Supply

FBVDD/Q PH1-4 OVR4+/OVR3I

1V8

Power Supply

1V8

5V

Power Supply

5V SWITCHER OVRU

PEX_VDD

Power Supply

PEX_VDD

Input Switch

OVRs

(RTD3 GC6 12V-OFF)

2xFAN

EXT_12V 2x4 PWR 1

EXT_12V 2x4 PWR 2

PEX_12V Finger

PEX_3V3 Finger

3V3_AUX Finger

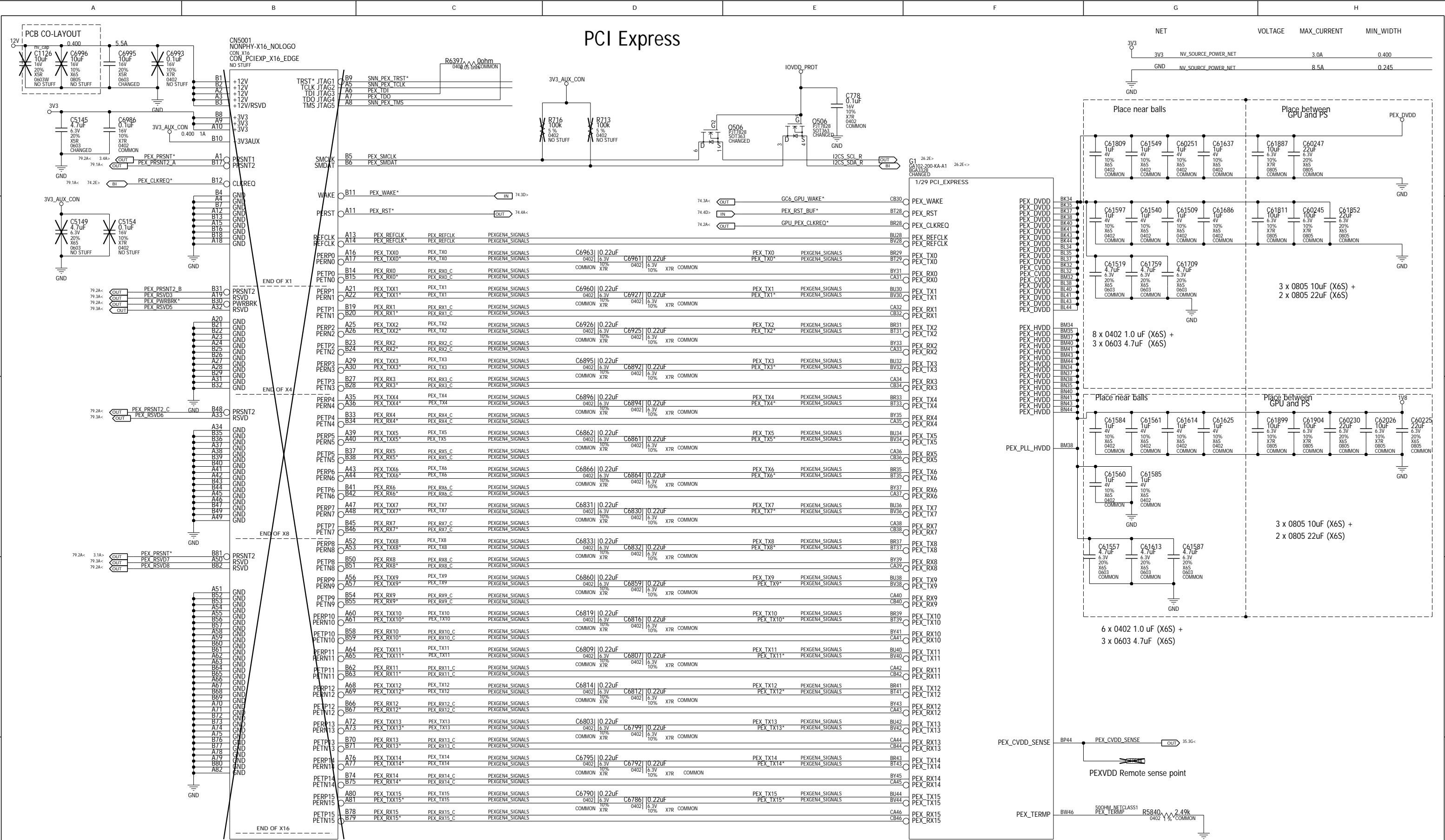
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BLOCK DIAGRAM

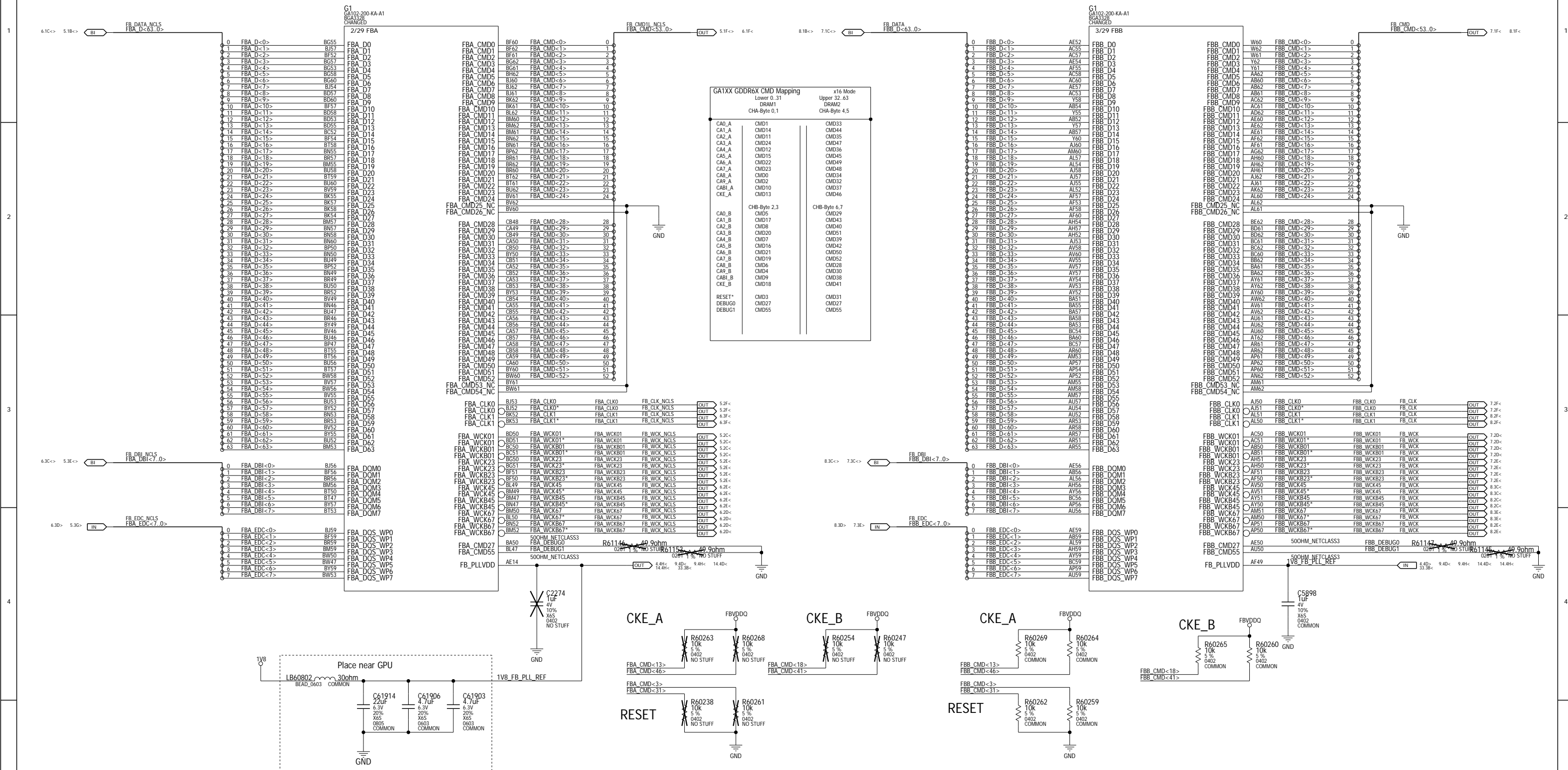
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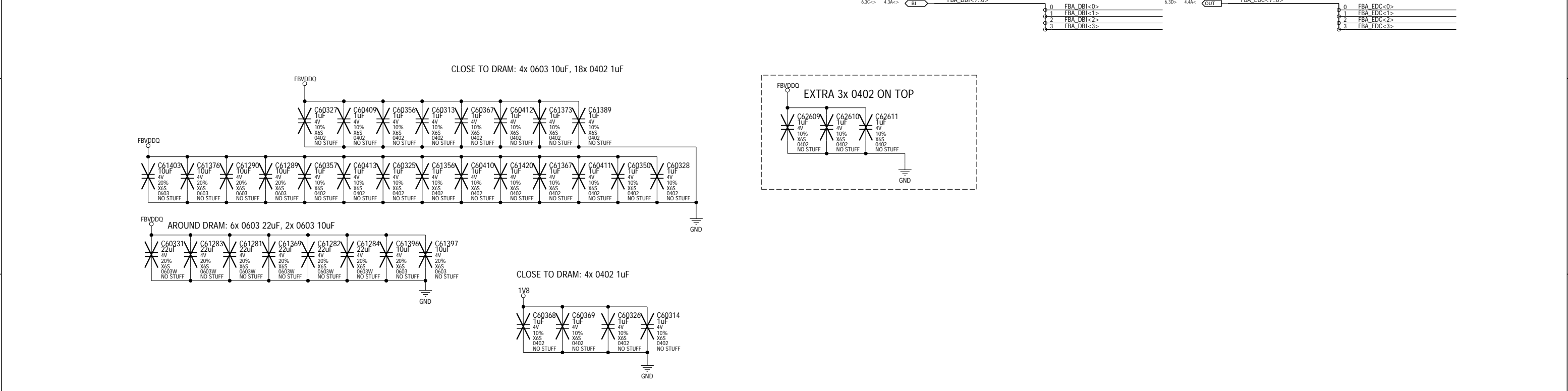



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MEMORY: GPU Partition A/B



[illegible]

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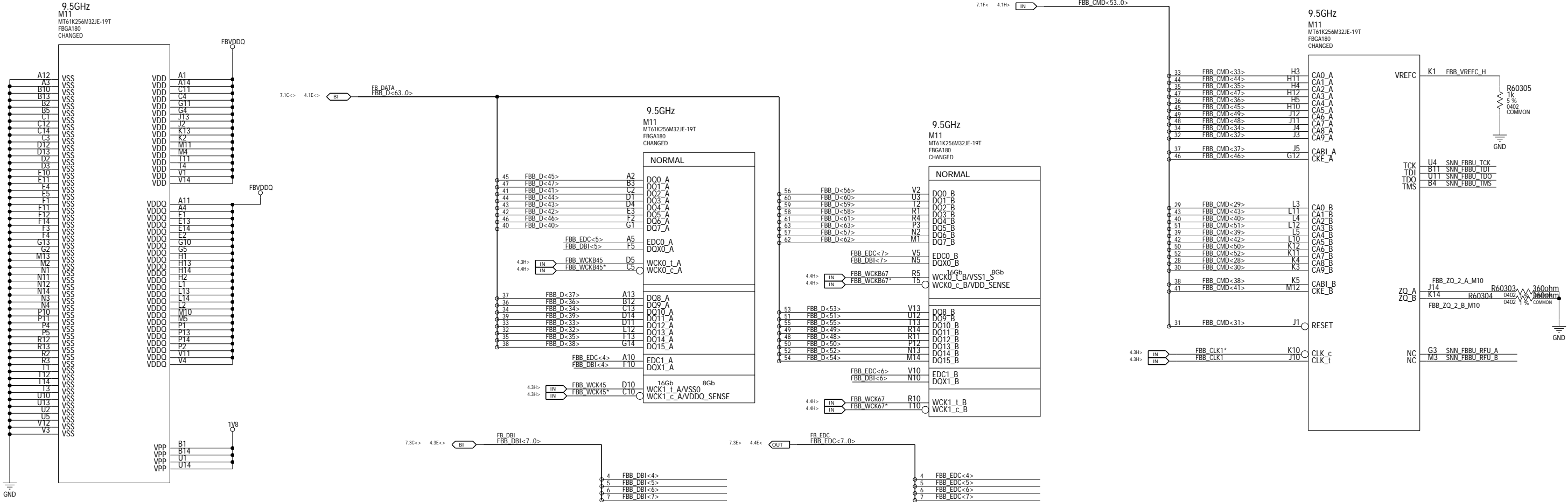
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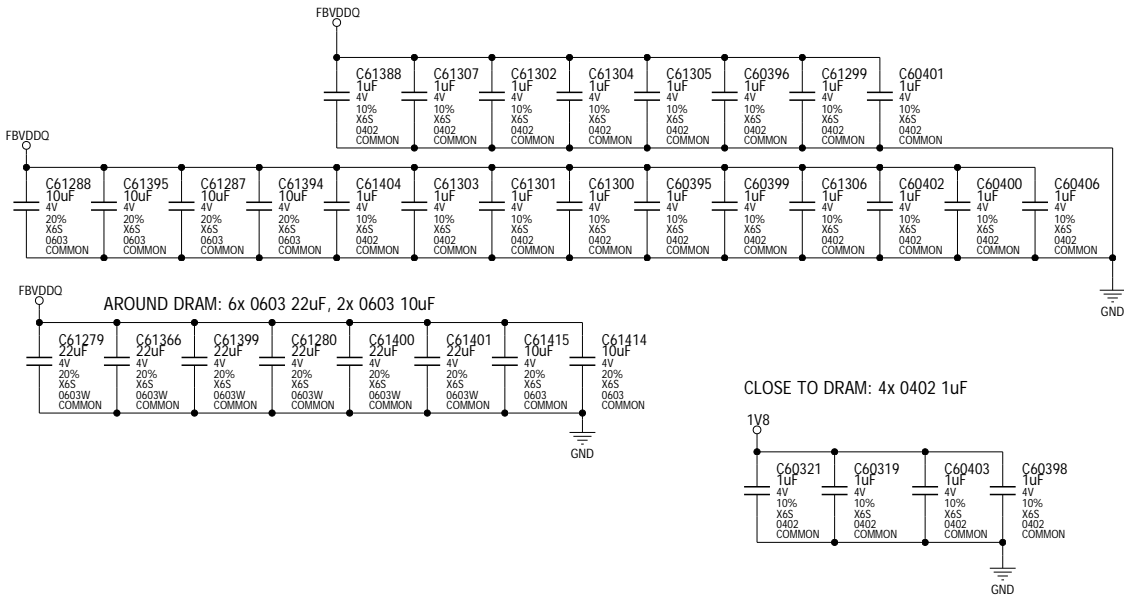
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MEMORY: FBB Partition 63..32



CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



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NV_PN 600-1G132-0030-300

PCB REV PG132-A02

BOM REV C

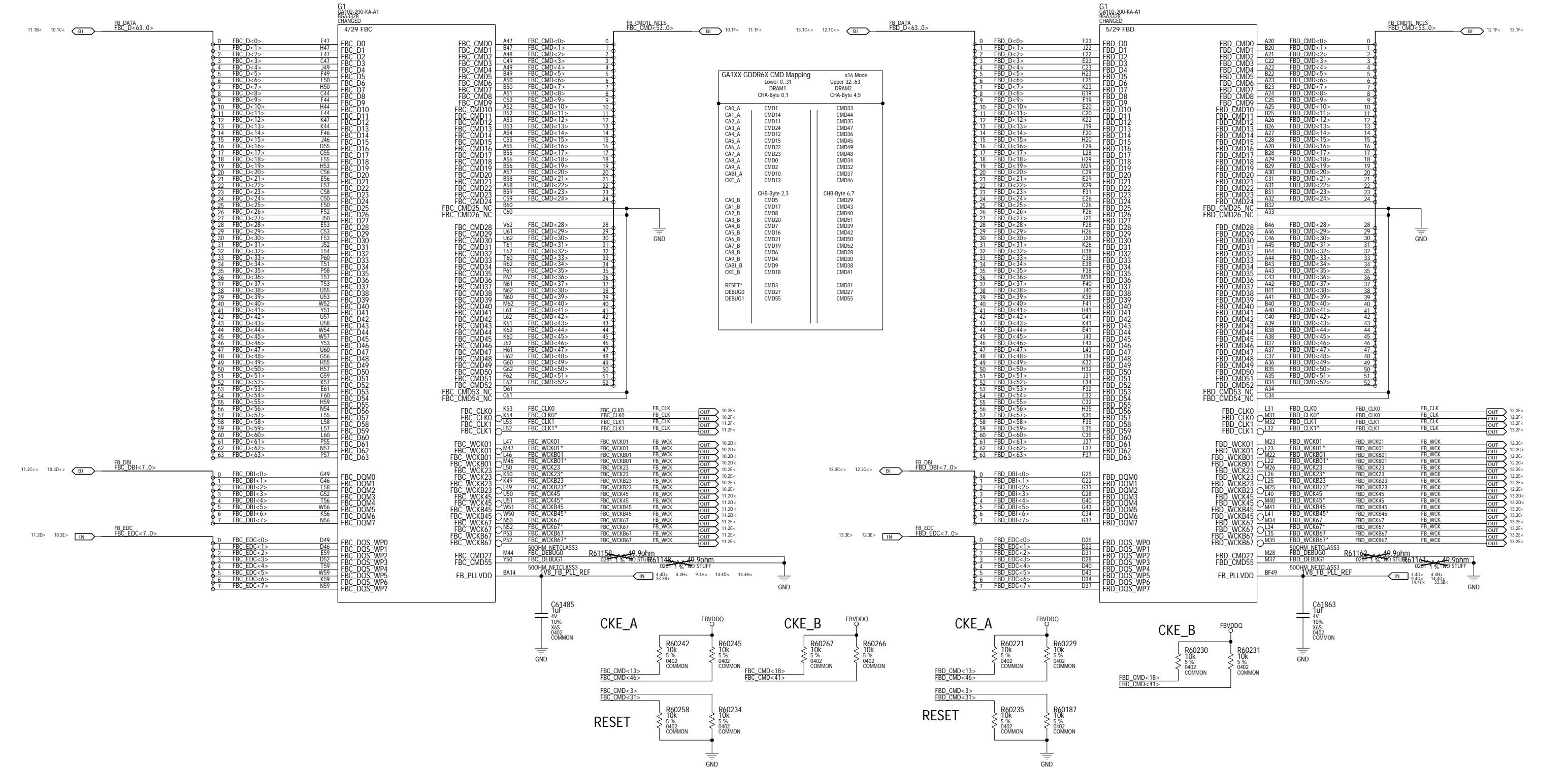
PAGE 8 OF 79

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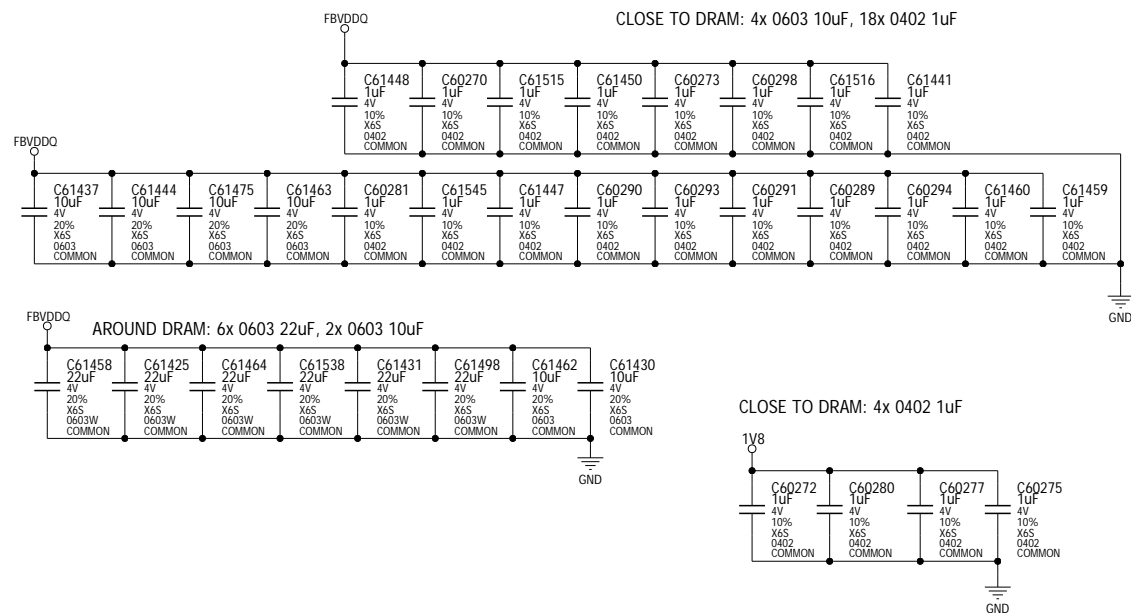
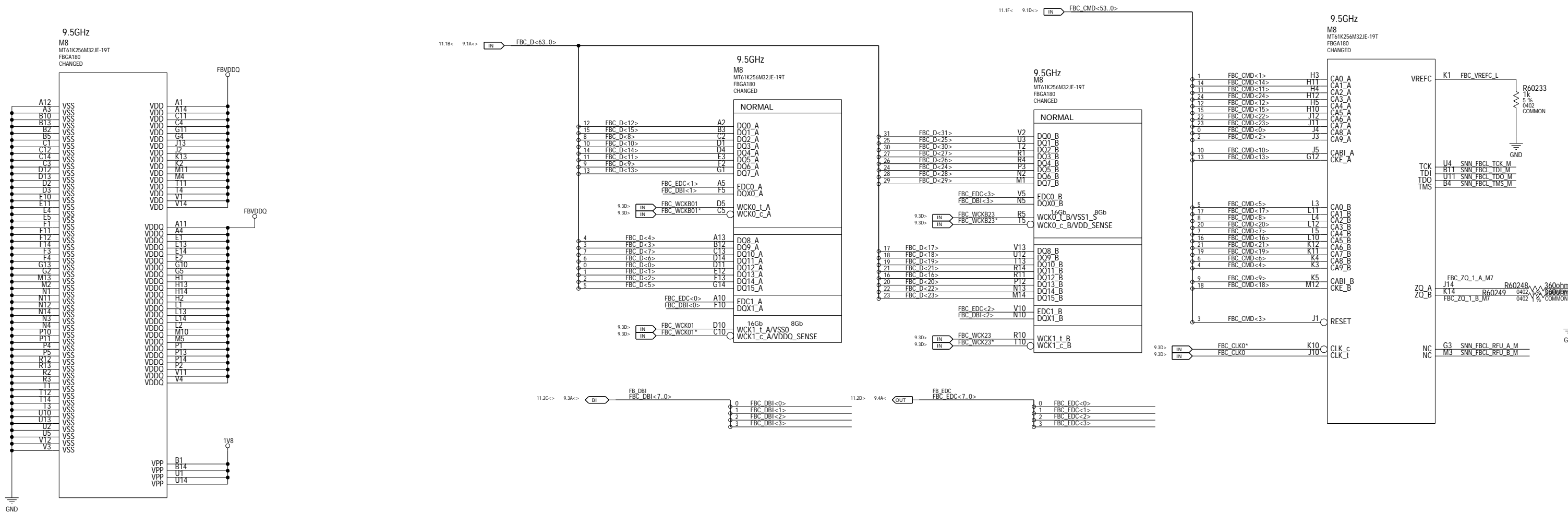
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PAGE DETAIL MEMORY: FBB PARTITION[63:32]

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MEMORY: GPU Partition C/D



MEMORY: FBC Partition 31..0



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: FBC PARTITION[31:0]

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PCB REV	PG132-A02
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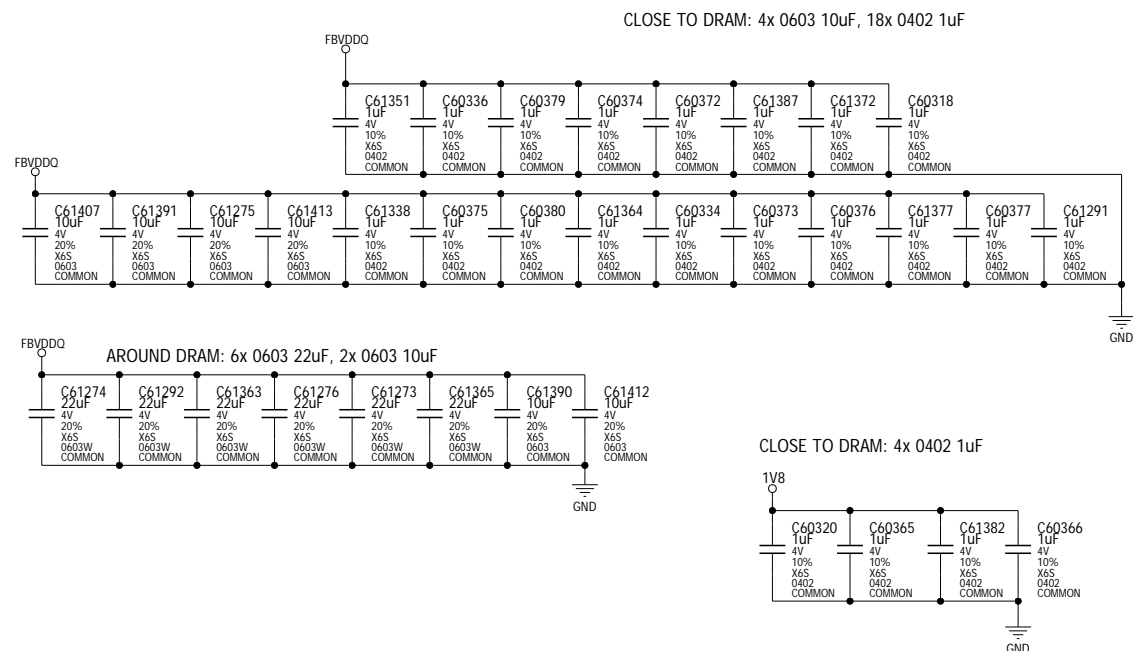
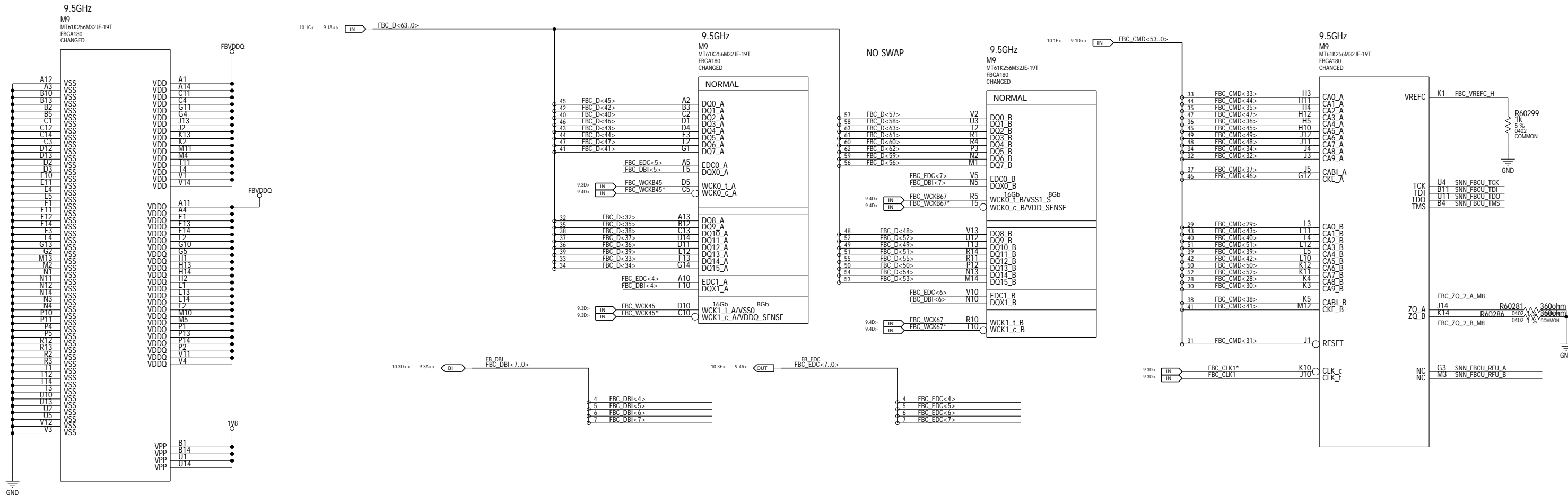
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MEMORY: FBC Partition 63..32



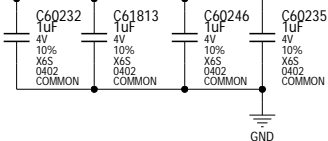
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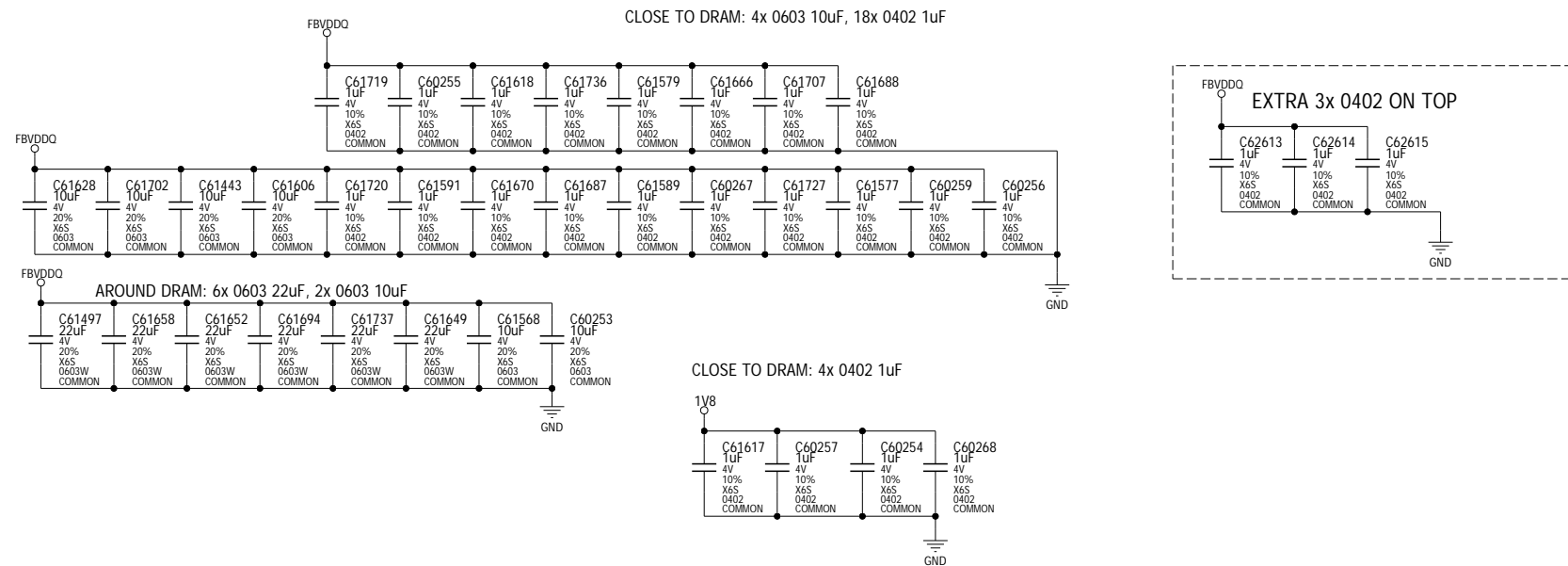
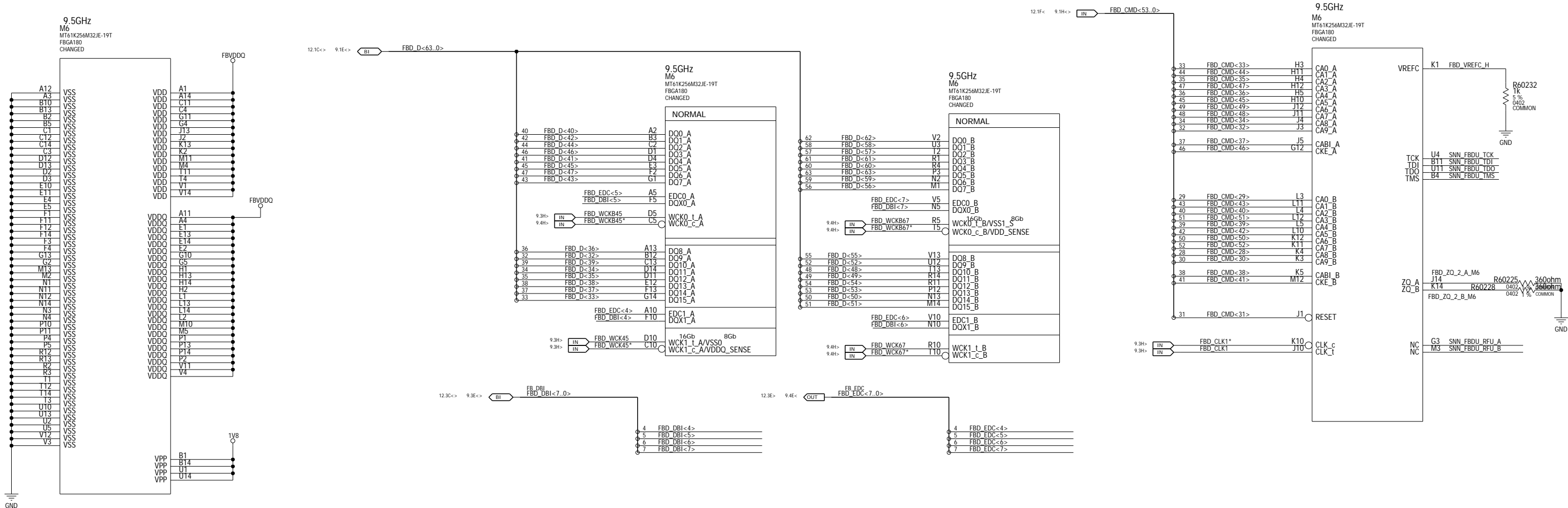
CLOSE TO DRAM: 4x 0402 1uF



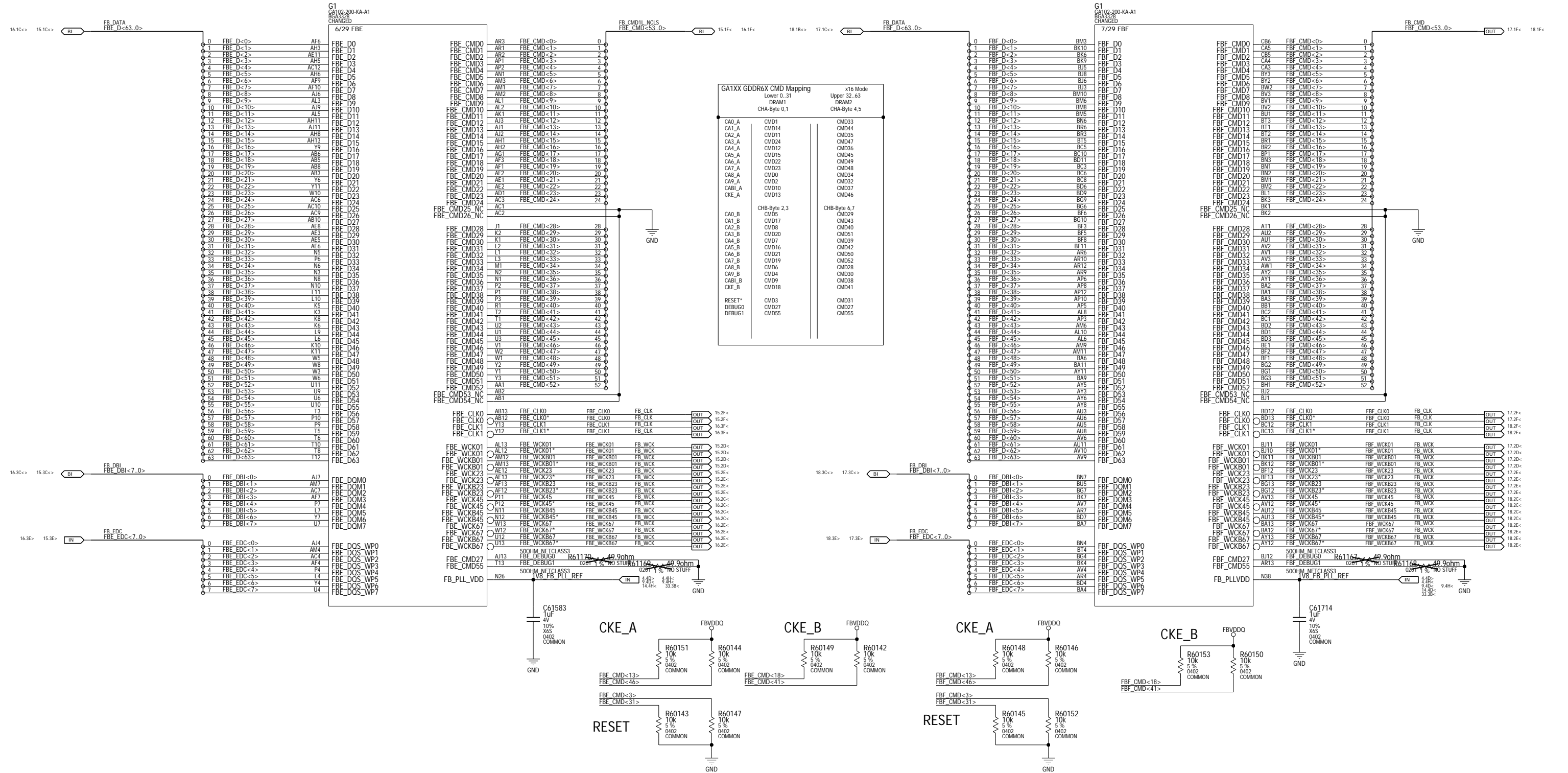
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MEMORY: FBD Partition 63..32

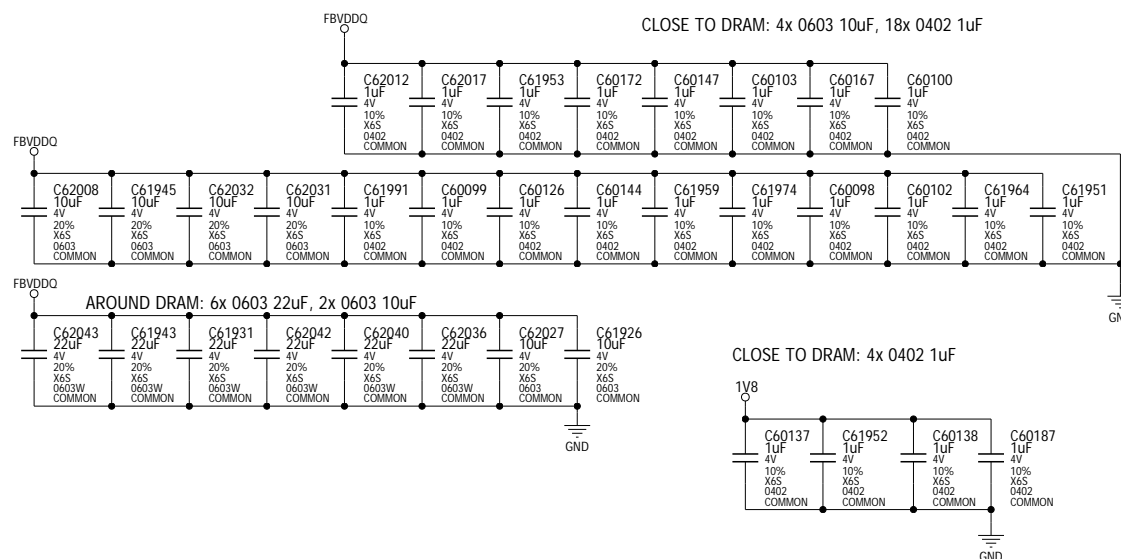
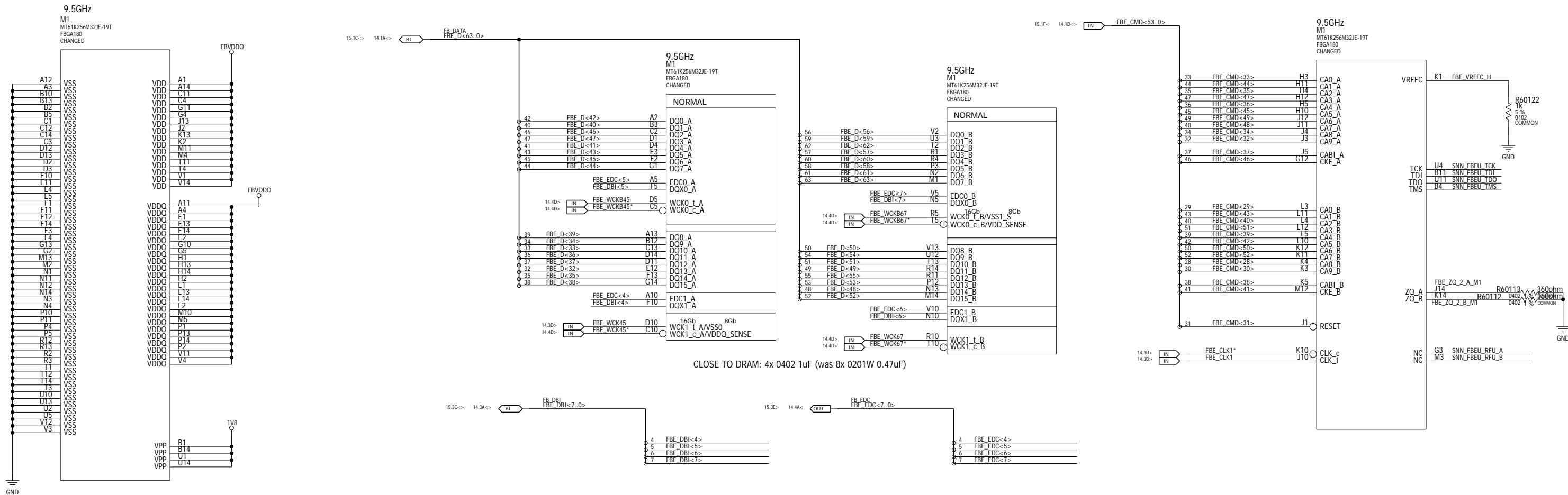


MEMORY: GPU Partition E/F



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MEMORY: FBE Partition 63..32

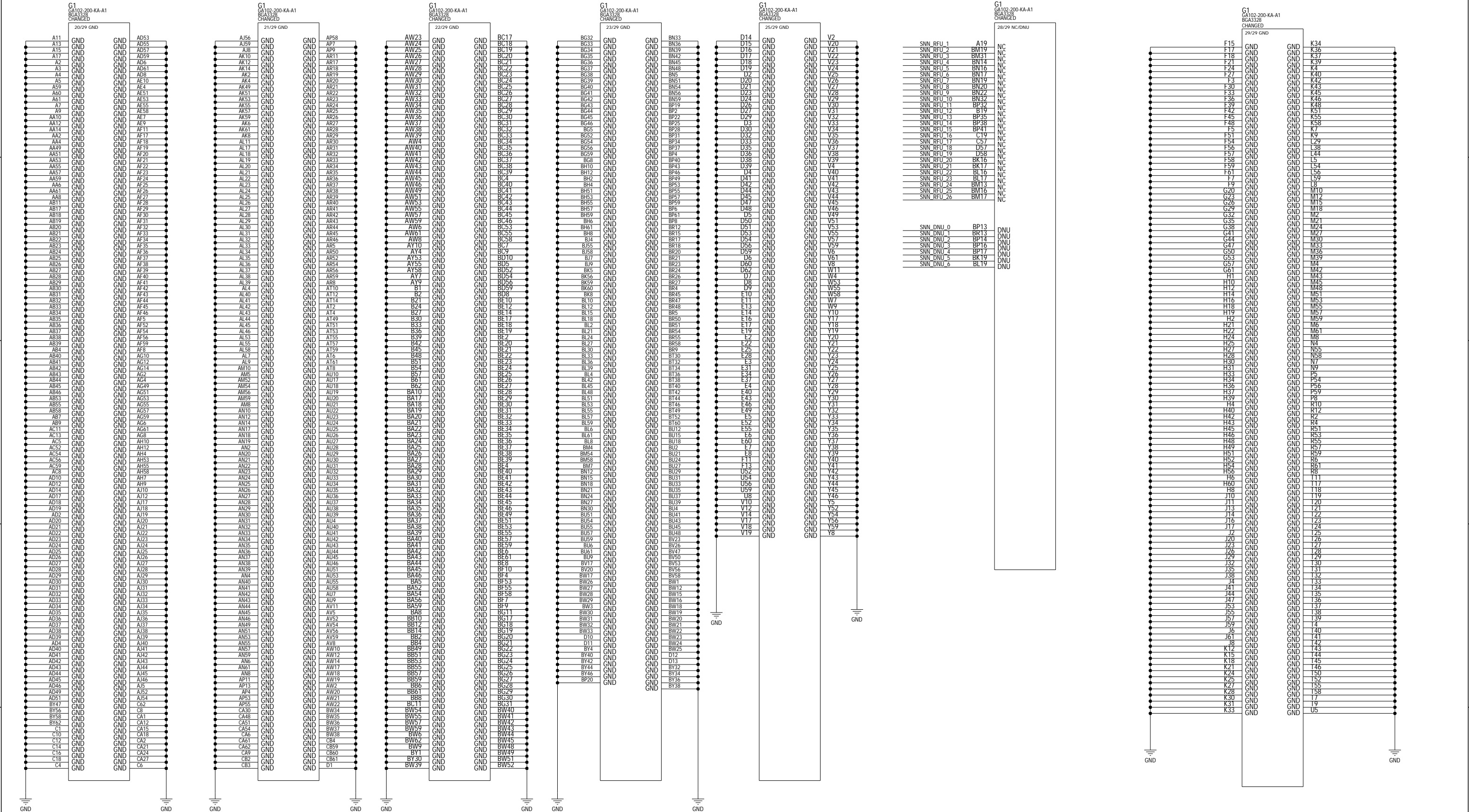


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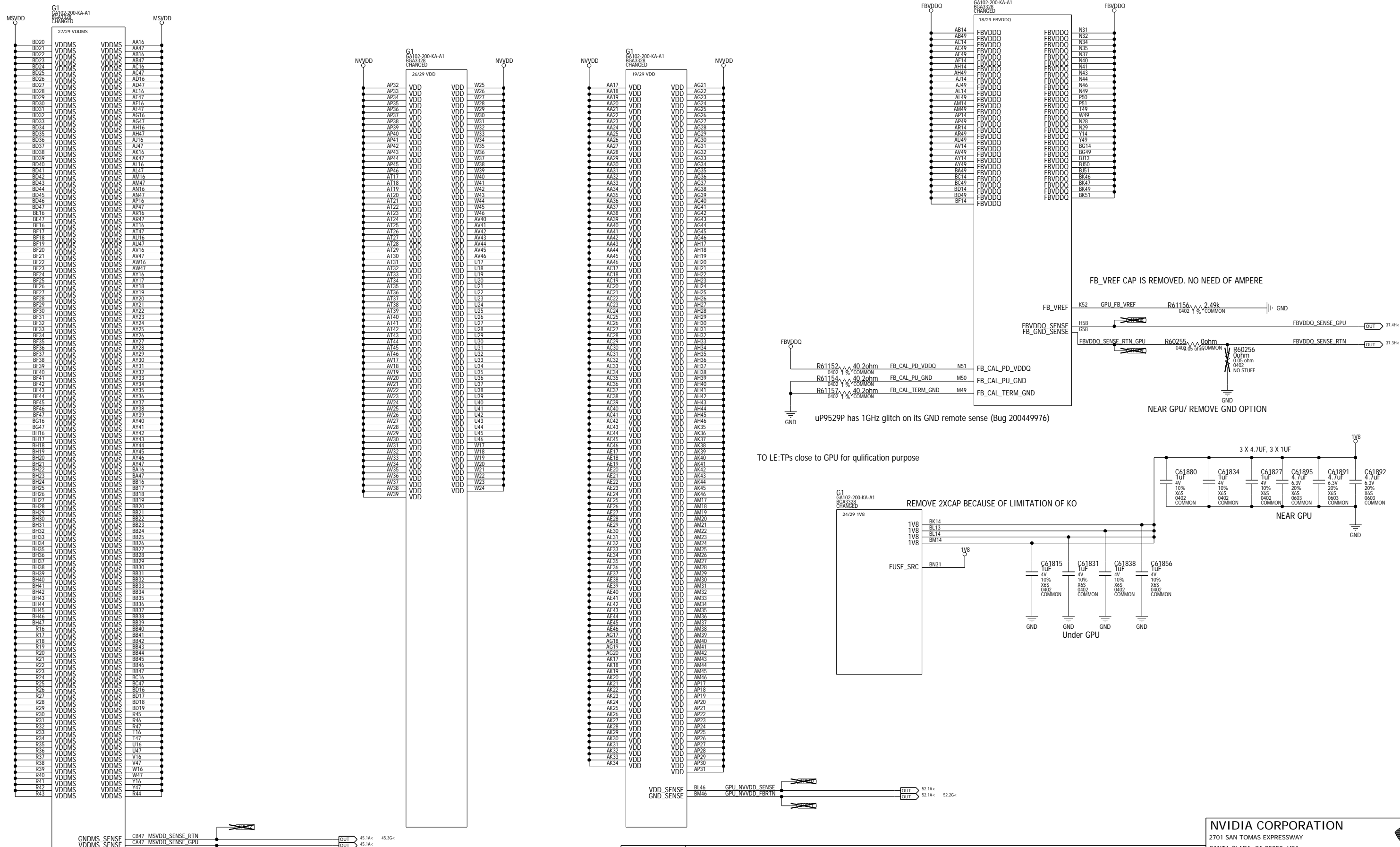
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GPU GND, RFUs & RSVD




GPU PWR and GND

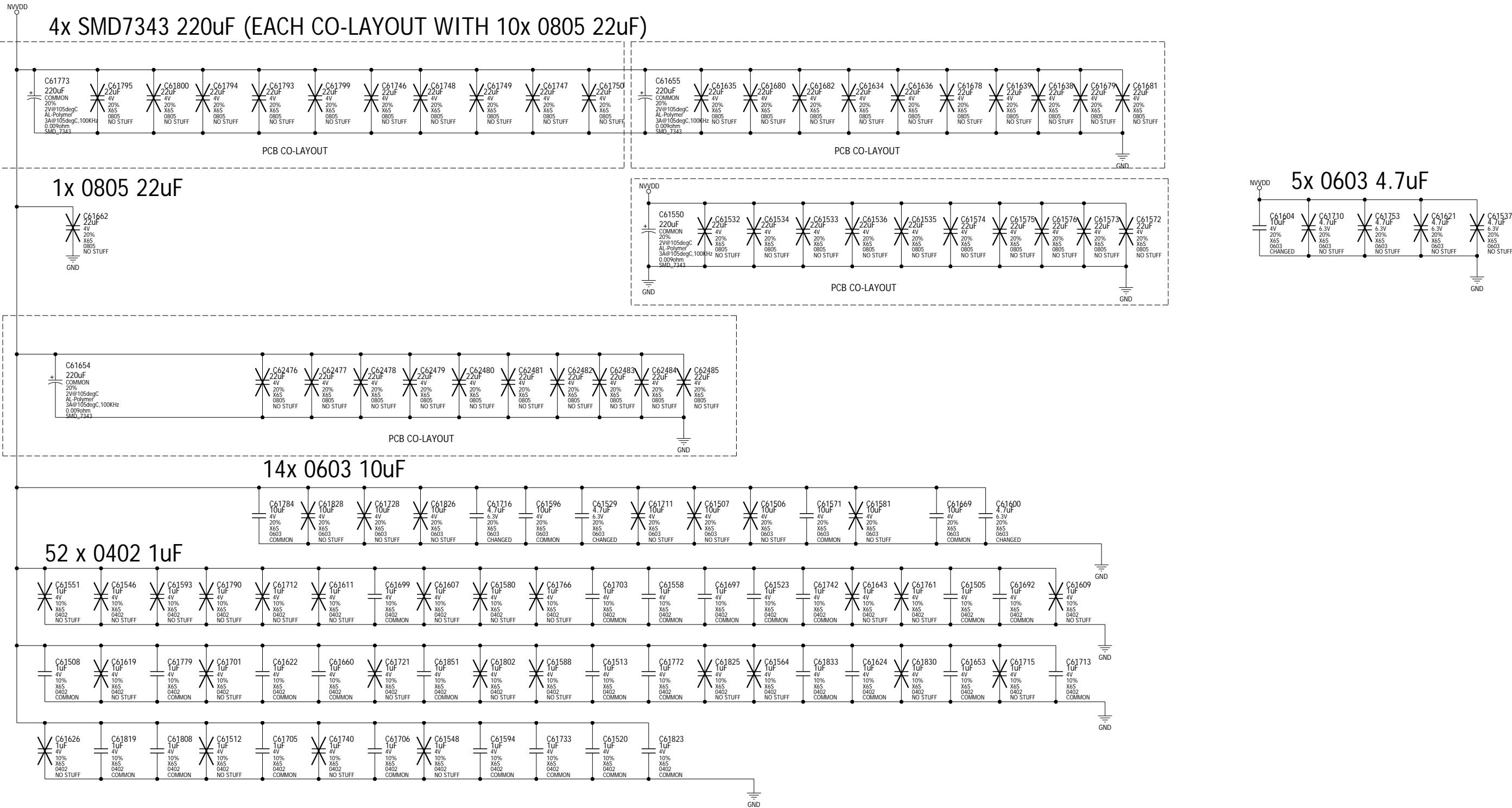


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PAGE DETAIL	GPU POWERS

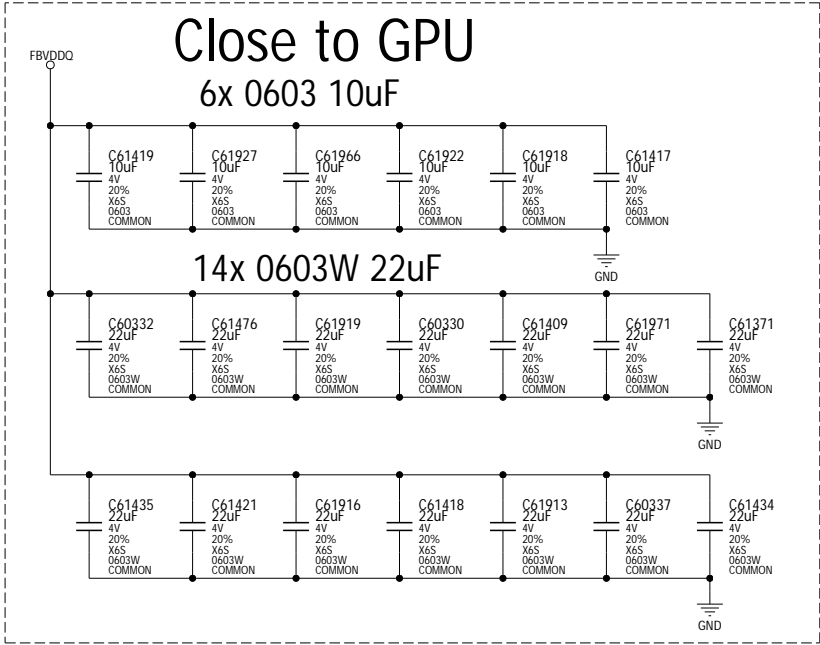
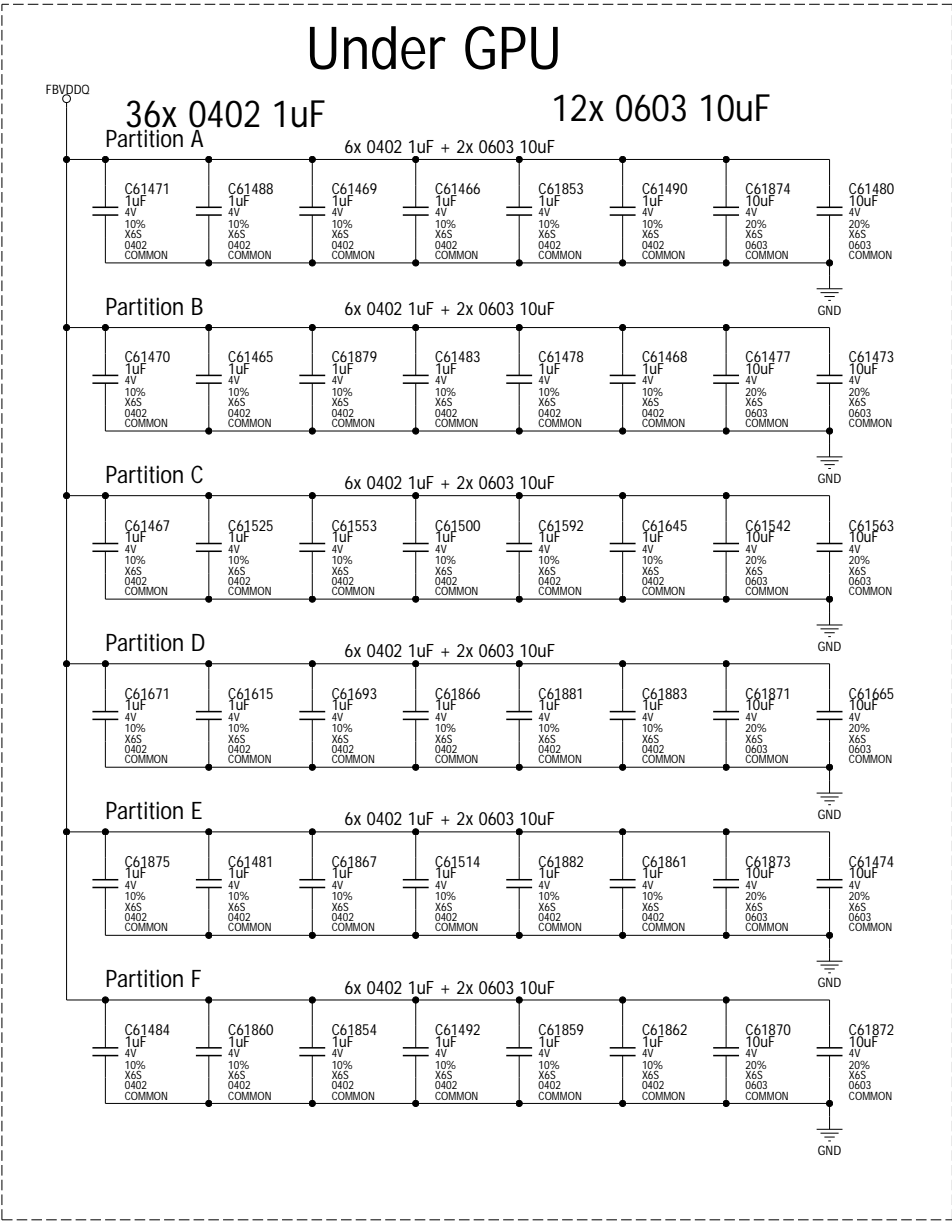
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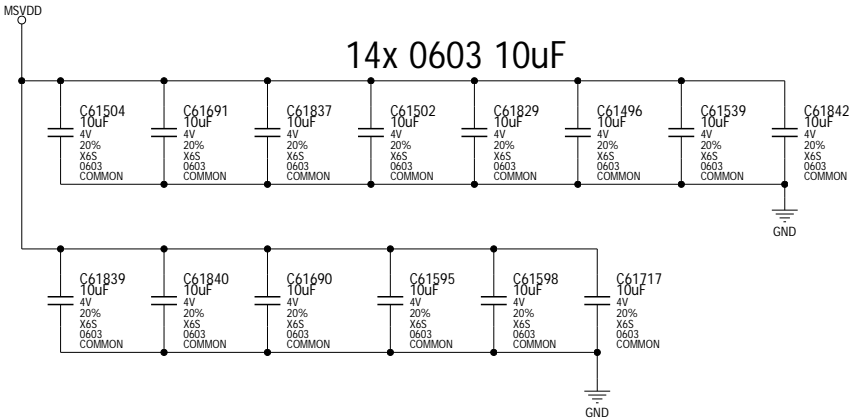
NVVDD UNDER GPU



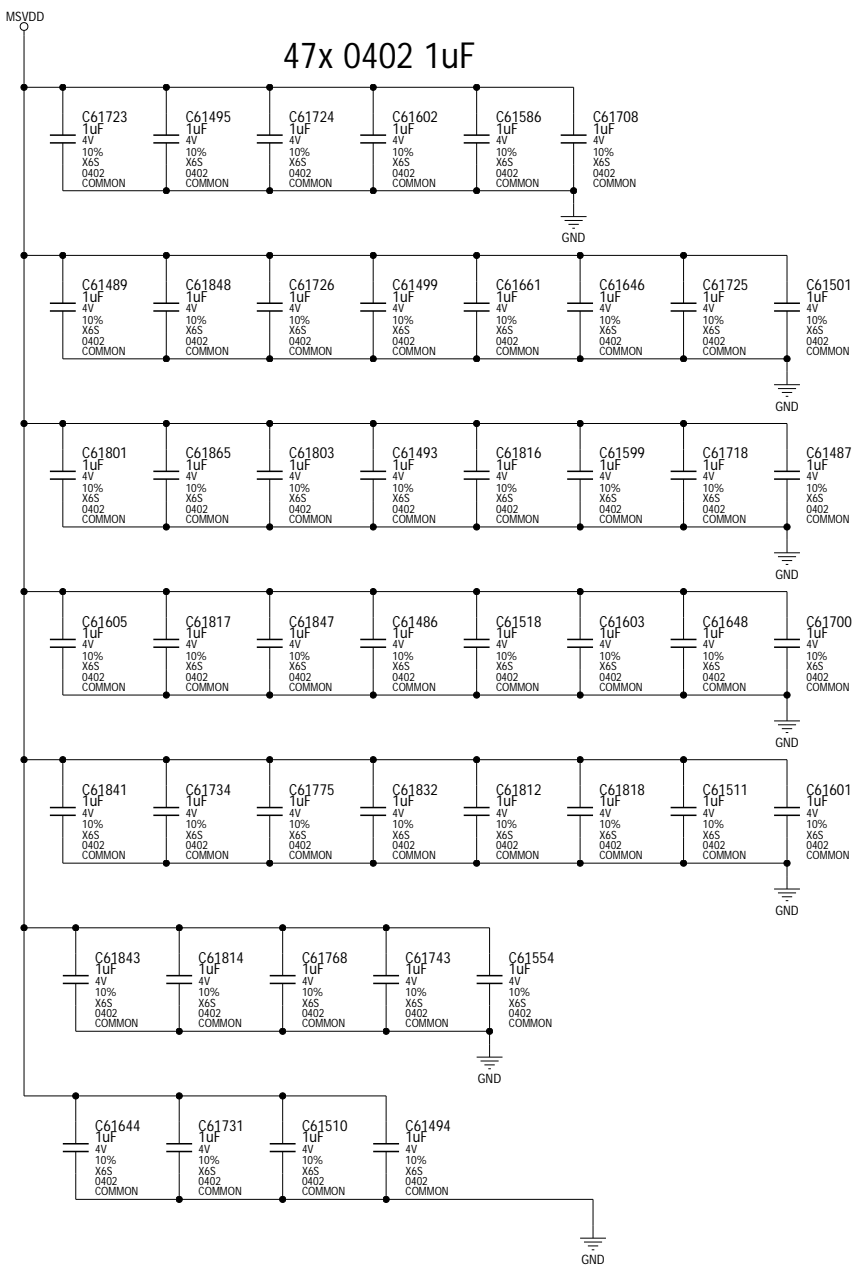
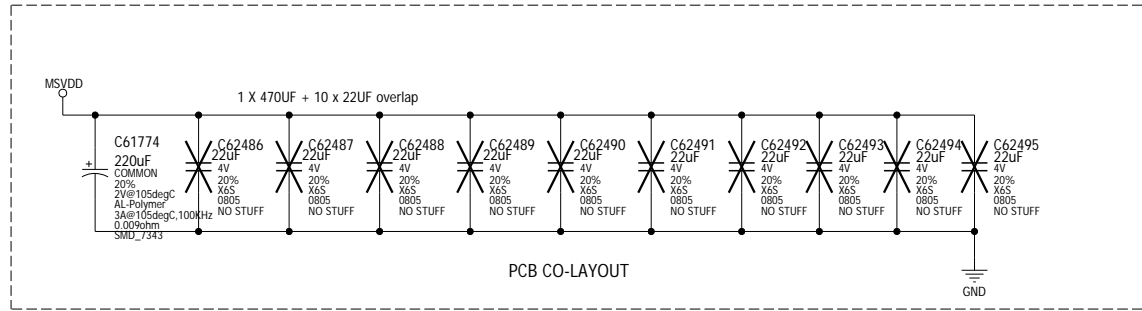
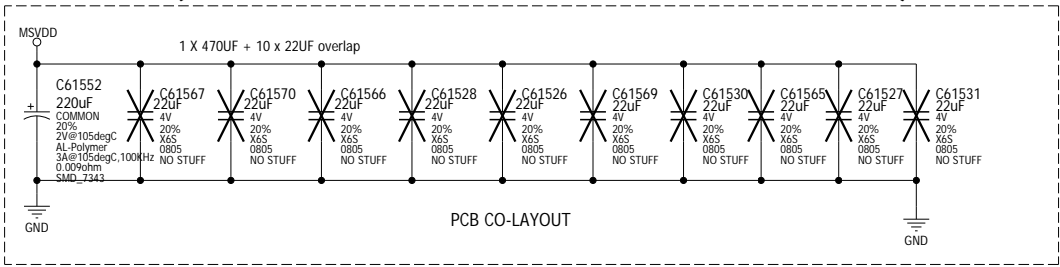
FBVDDQ



UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)

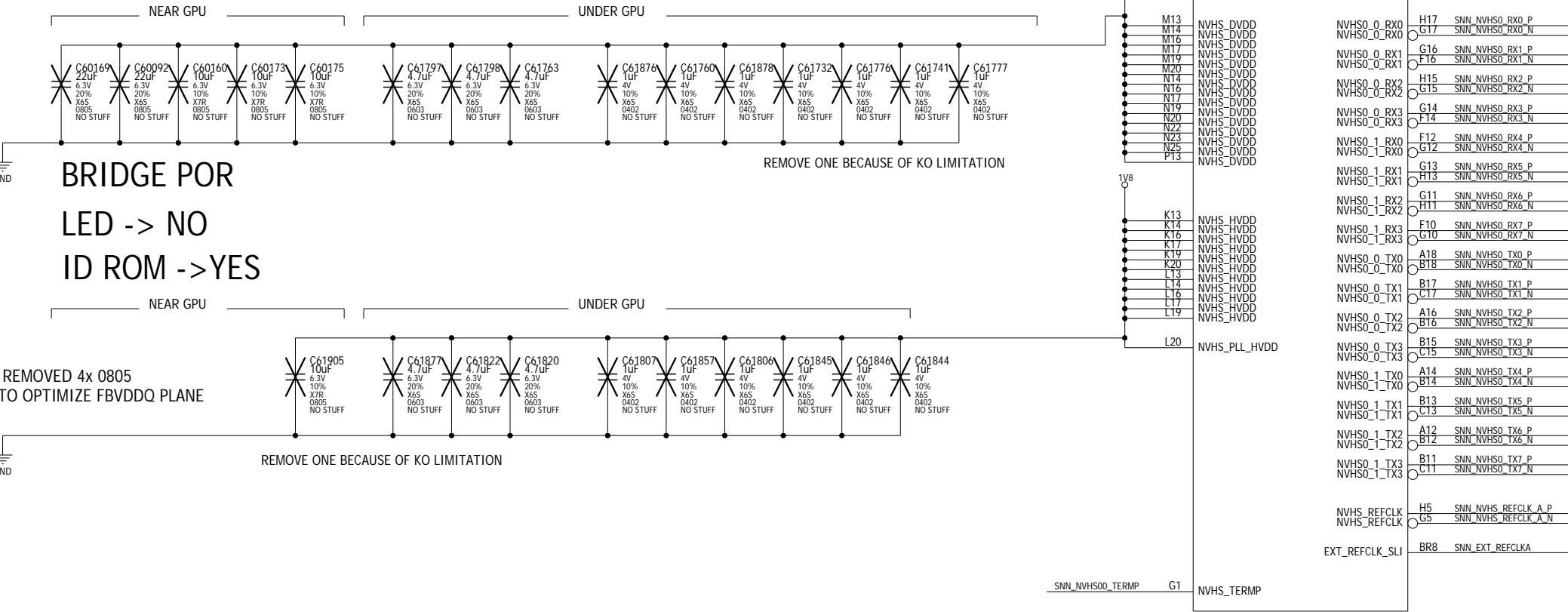


REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION



BLANK

NVHS Interface and FRAME LOCK



BRIDGE POR
LED -> NO
ID ROM -> YES

REMOVED 4x 0805
TO OPTIMIZE FBVDDQ PLANE

REMOVE ONE BECAUSE OF KO LIMITATION

REMOVE ONE BECAUSE OF KO LIMITATION

SHARE CAP WITH NVHS_DVDD

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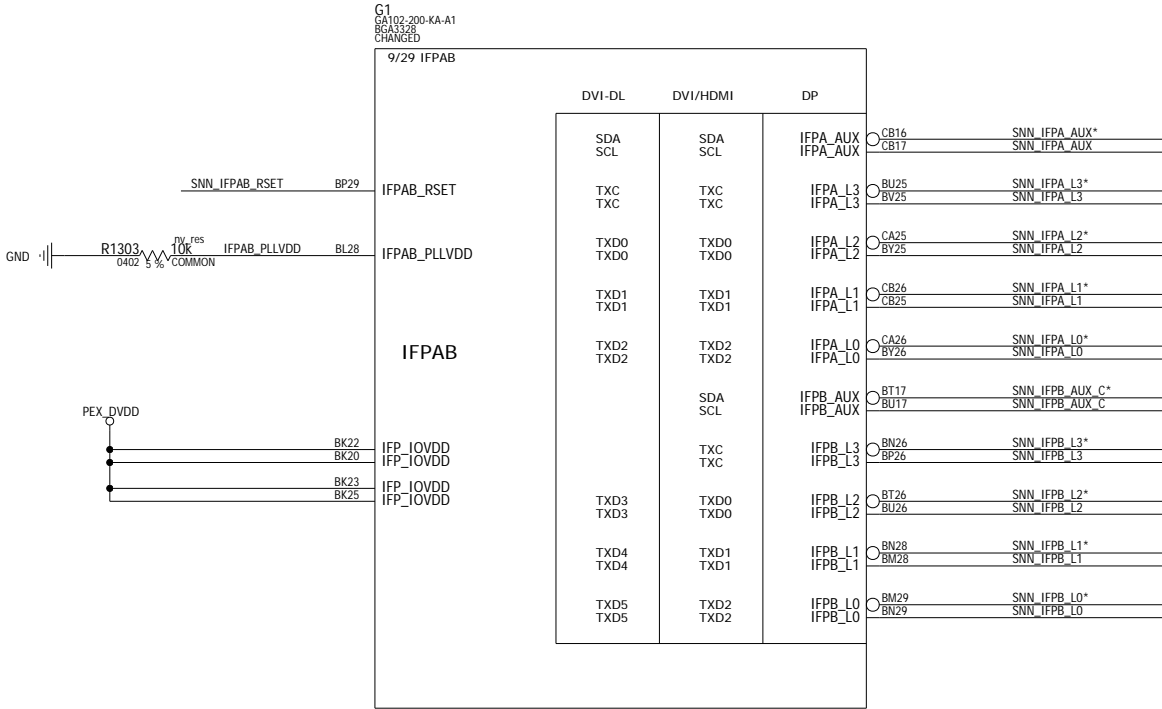
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IFPA UNUSED, IFPB UNUSED



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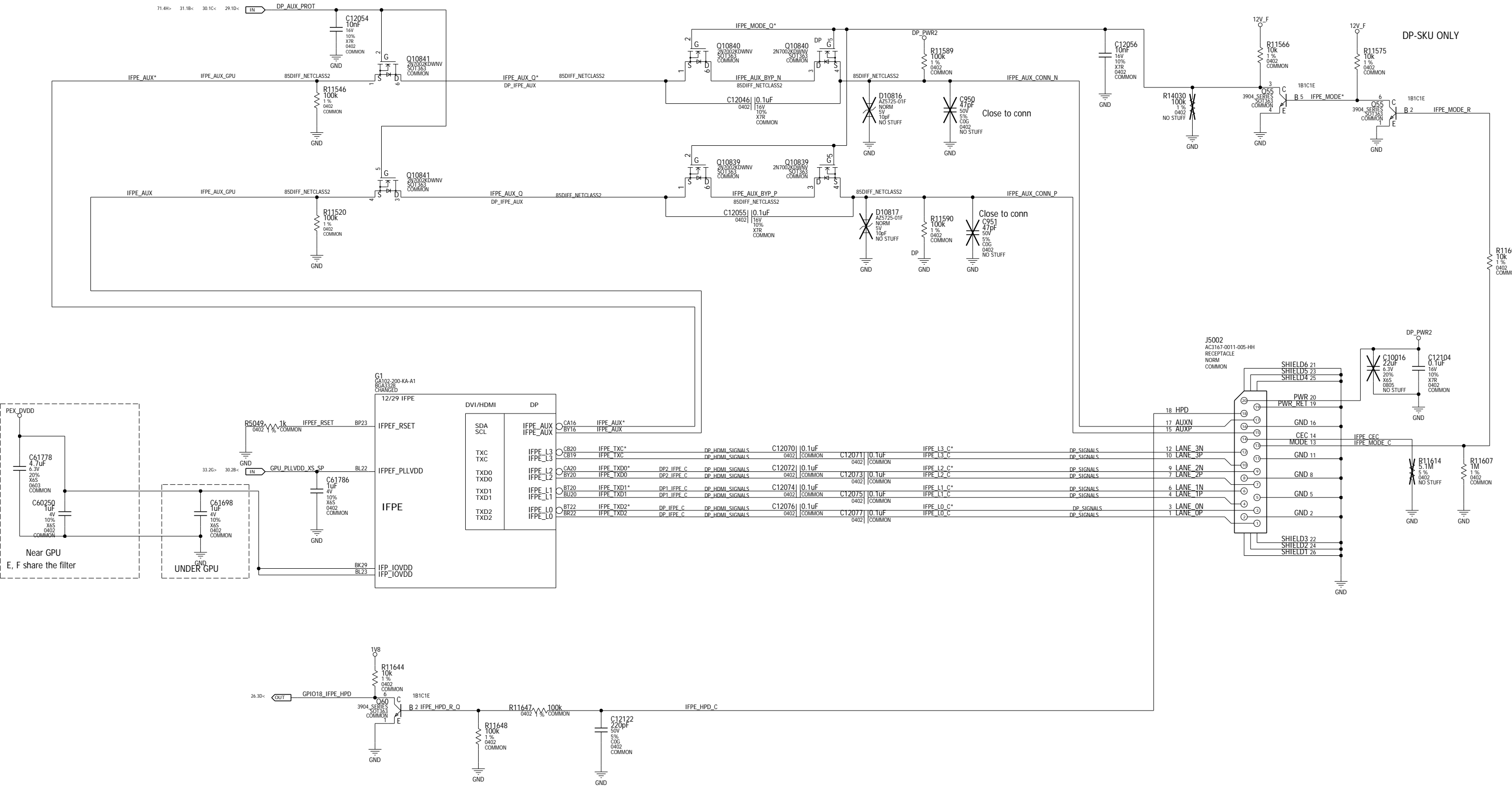
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IFPE DP



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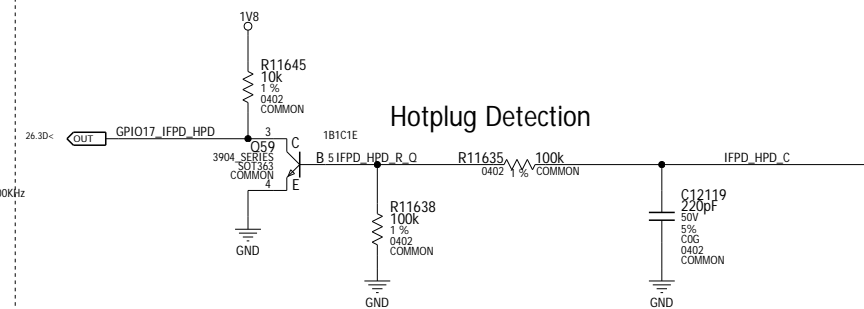
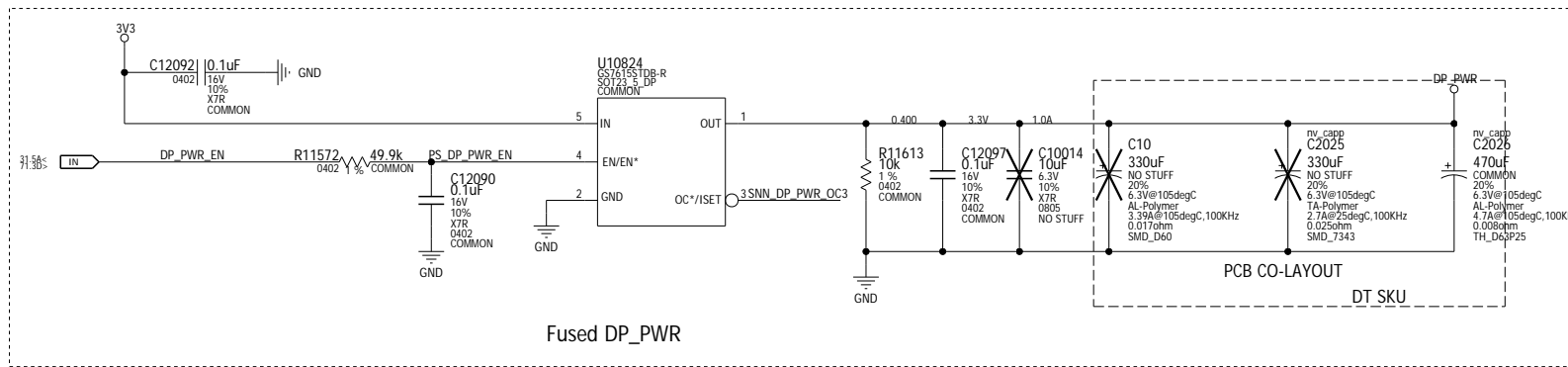
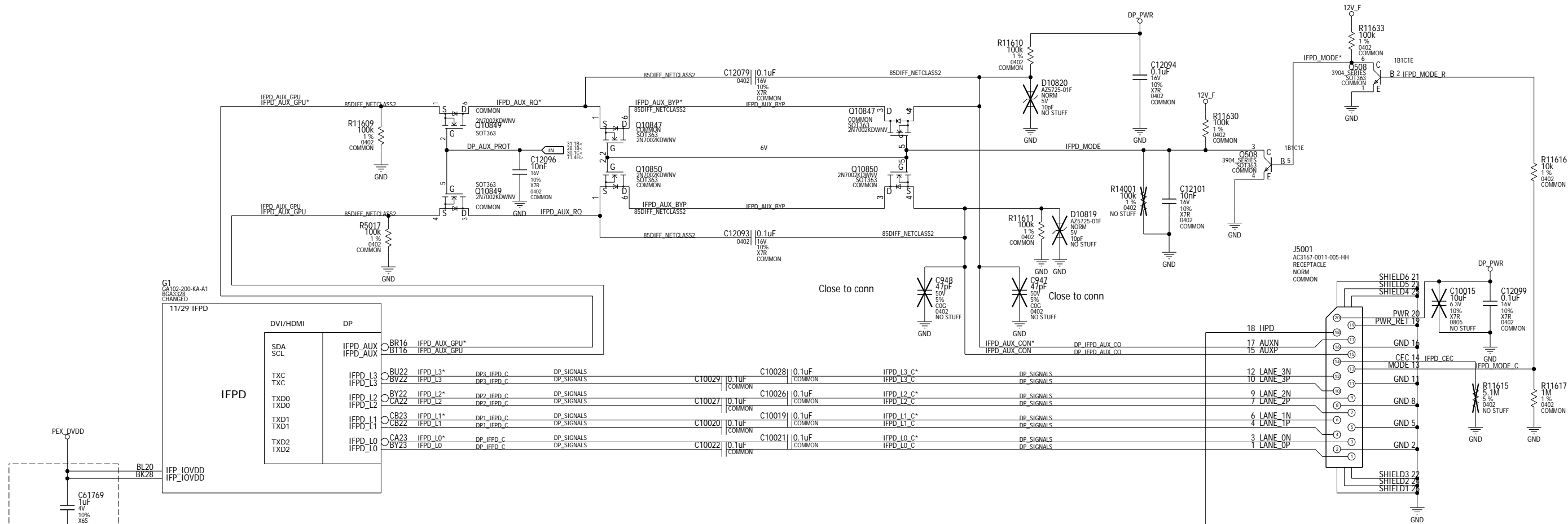
BOM REV C

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPE DP

IFPD DP



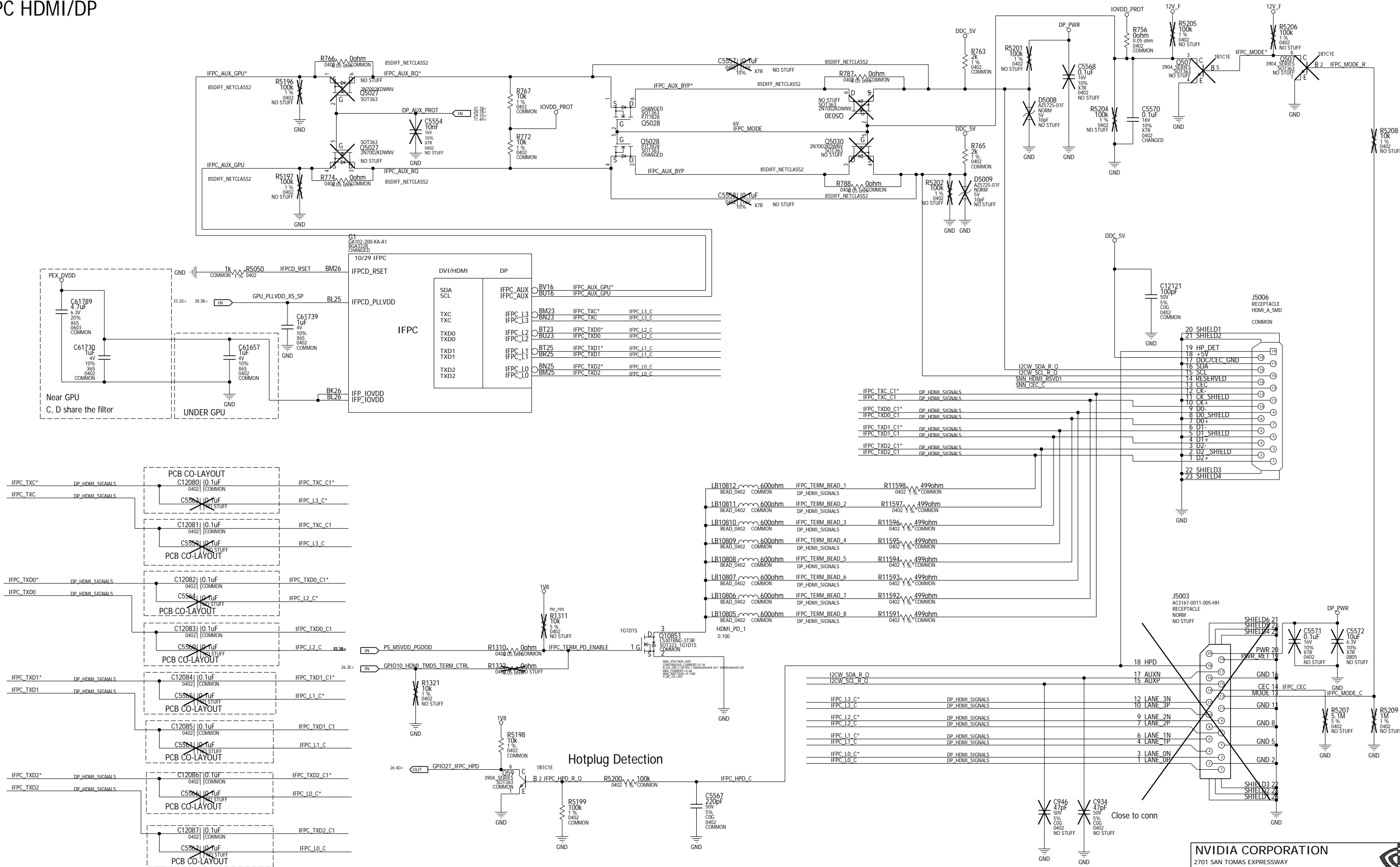
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IFPC HDMI/DP



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PAGE DETAIL	IFPC HDMI/DP

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MISC: ROM, Straps

GROUP0 STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
H	H	H	0111	FS_OVERT ENABLE	DEFAULT
L	L	L	0000	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	Default

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

<-A01 PCB

<-OLD

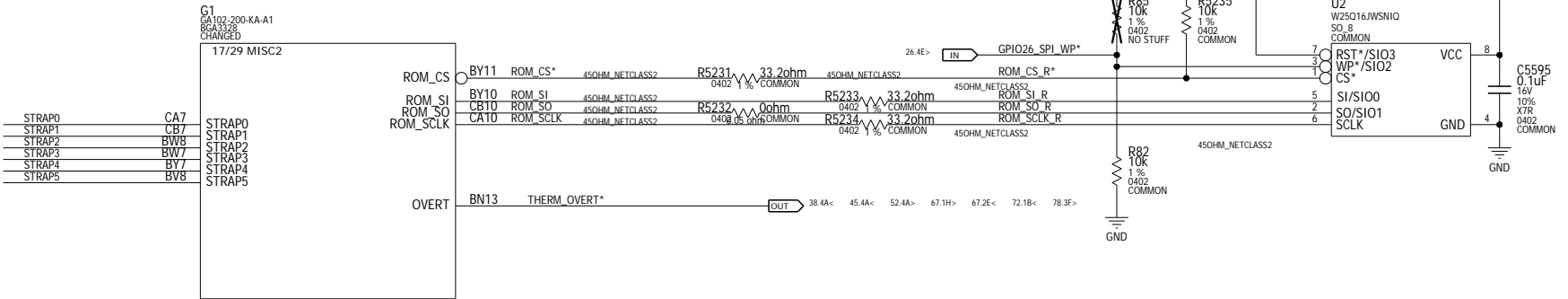
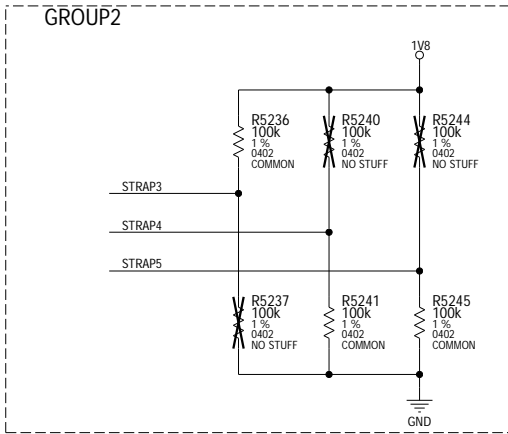
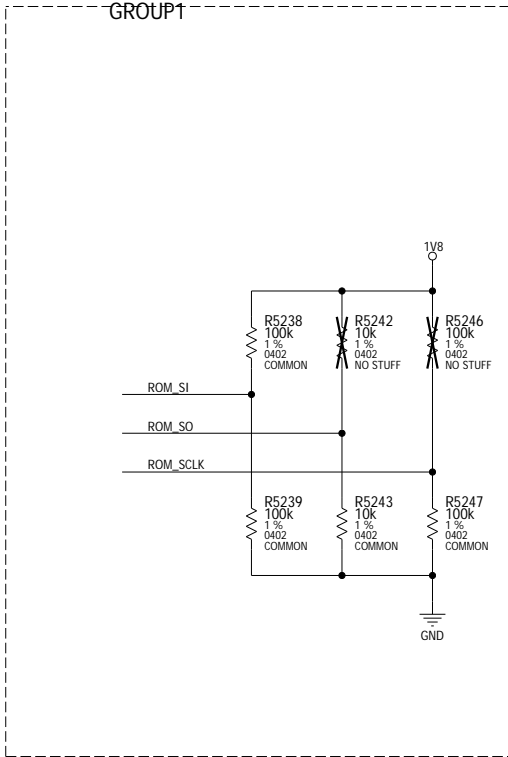
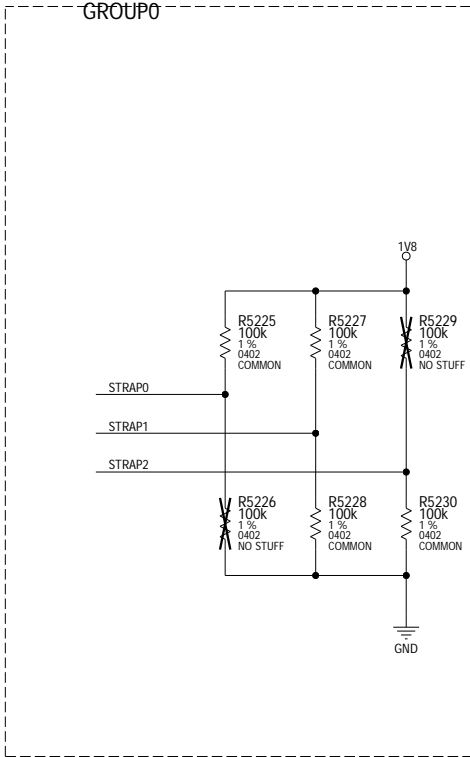
<-LATEST A02 PCB

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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PCB REV PG132-A02

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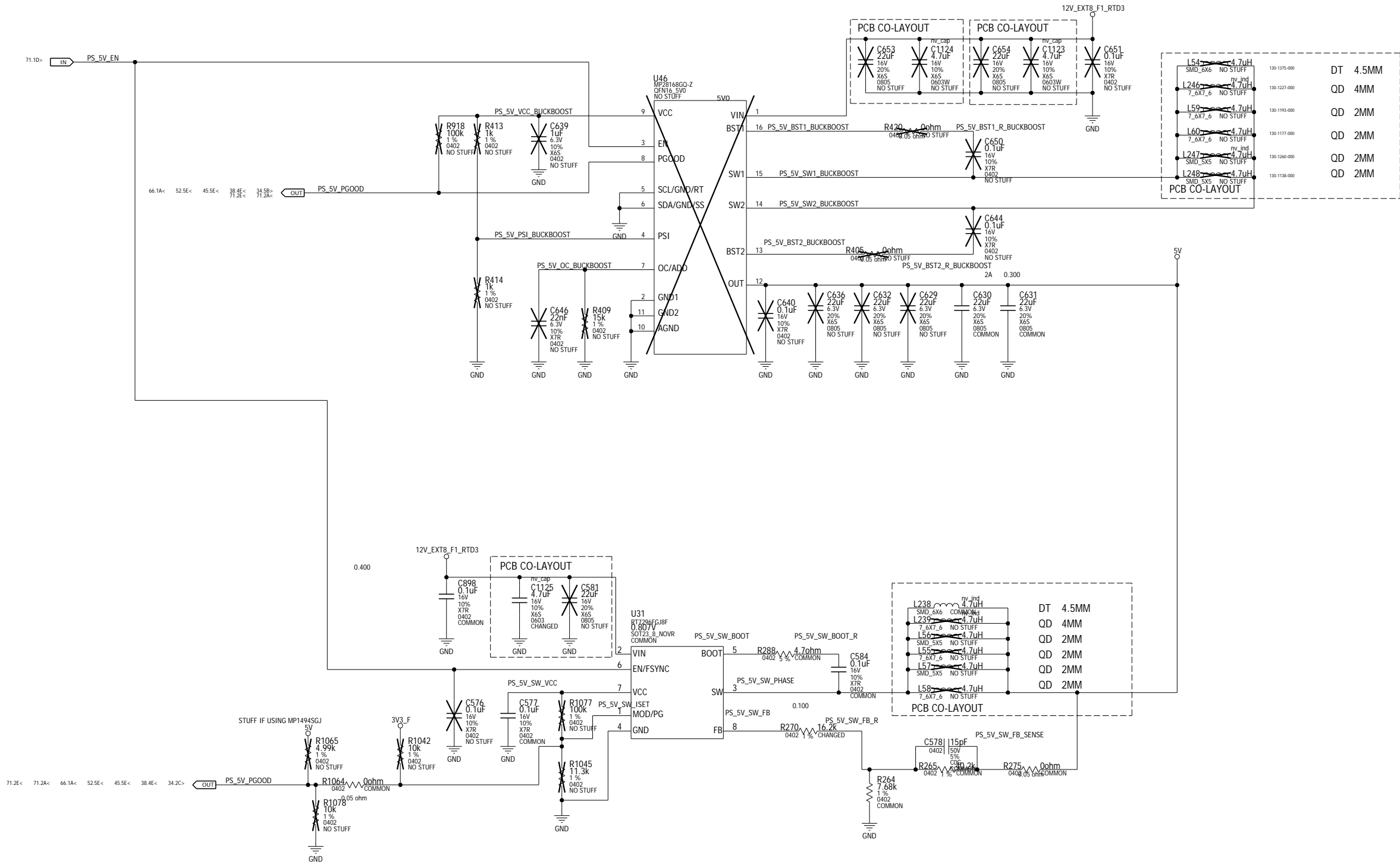
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PS: 5V, 5V_BACKUP



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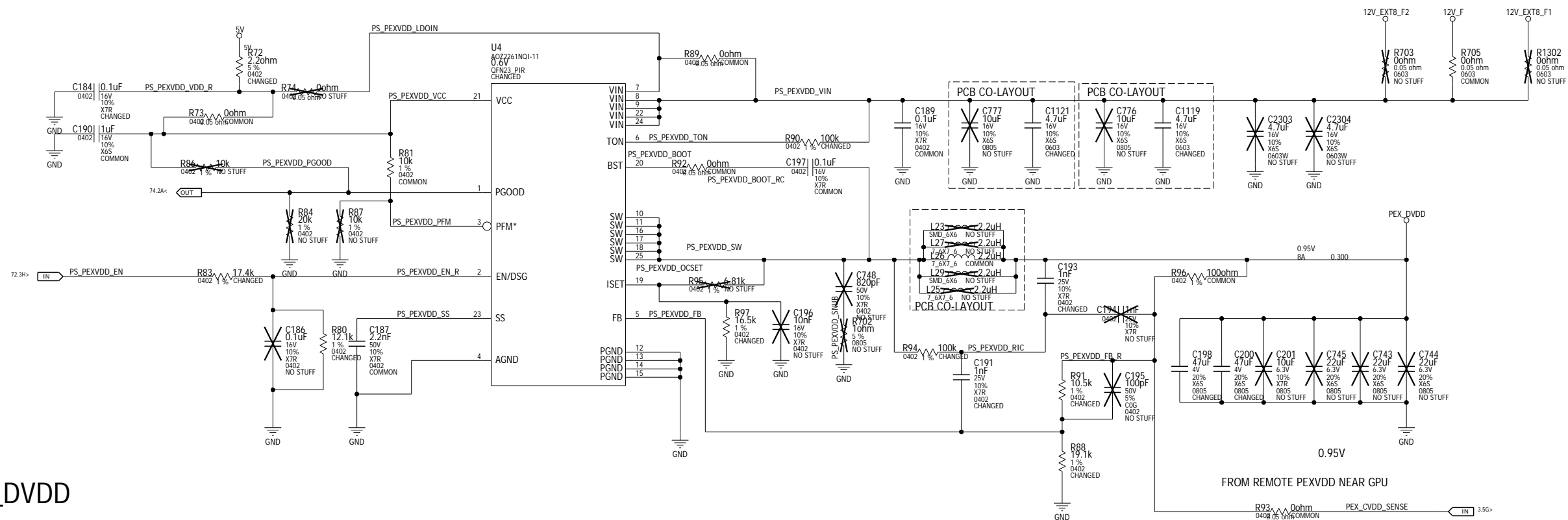
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BOM REV C

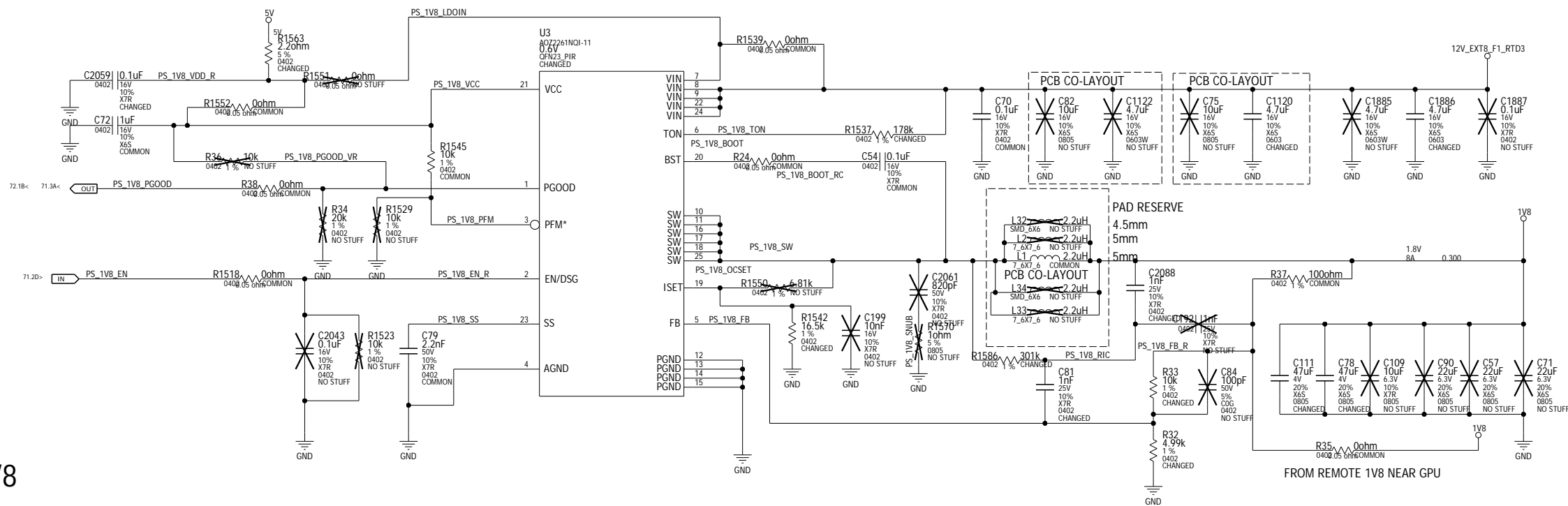
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PS: PEX_DVDD 1V8 Rail



PEX_DVDD



1V8

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: PEX_DVDD and 1V8

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BOM REV

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DATE	15-JUN-2020
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PIN12 MP2988 VIN SENSE 1/16 DIVIDER
PIN12 UP9529 REFOUT

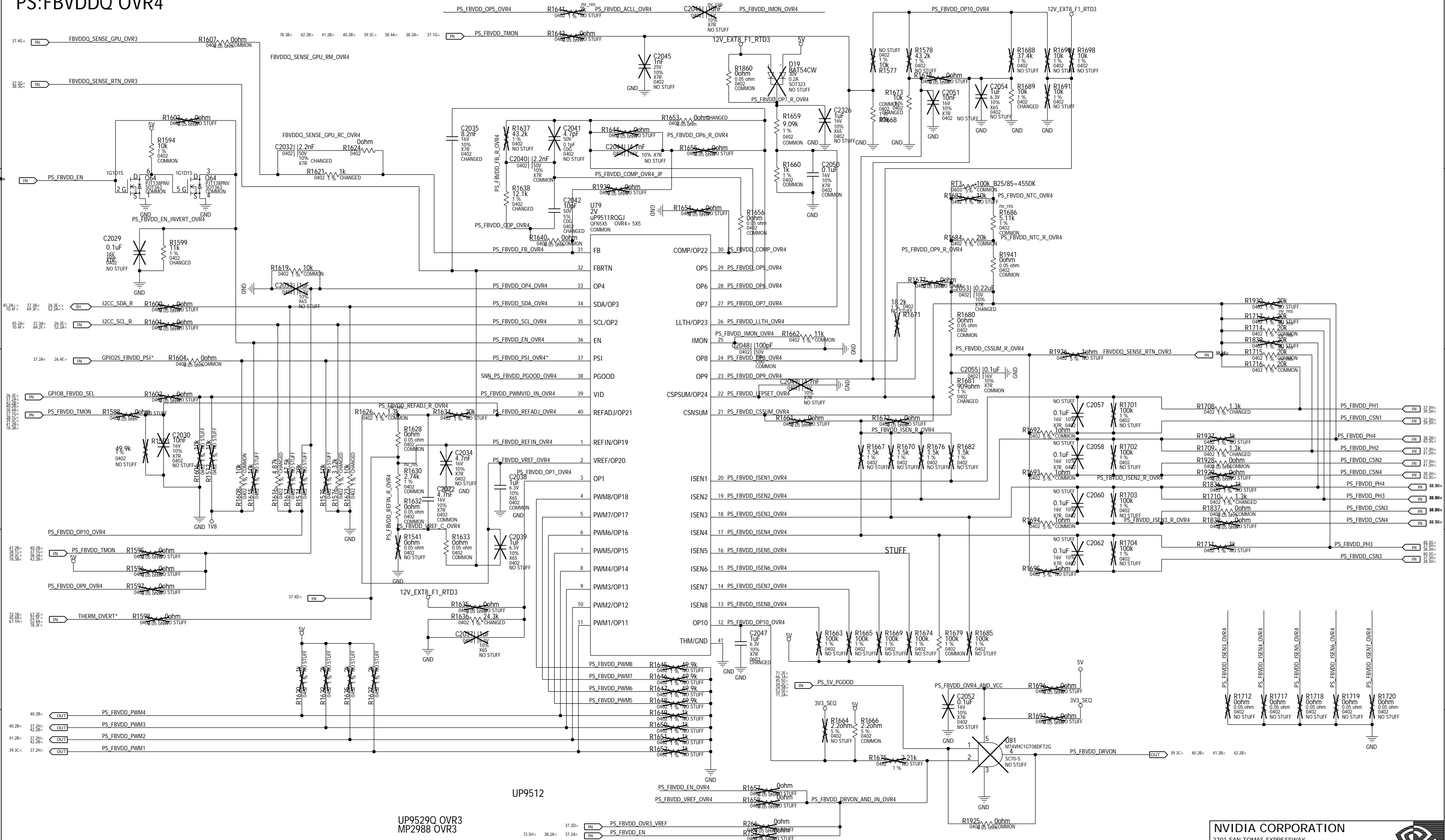


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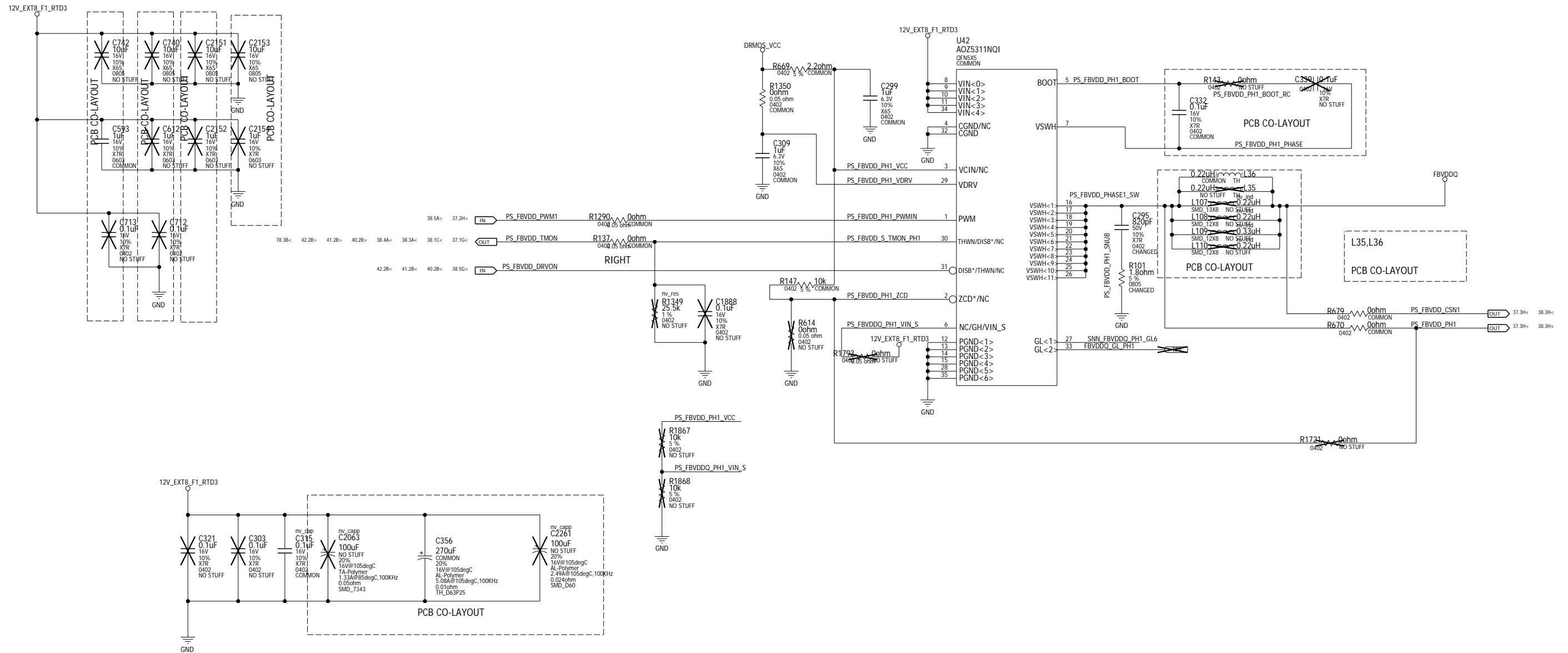


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PS:FBVDDQ OVR4



PS: FBVDD PH1



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PAGE DETAIL	PS: FBVDD PH1

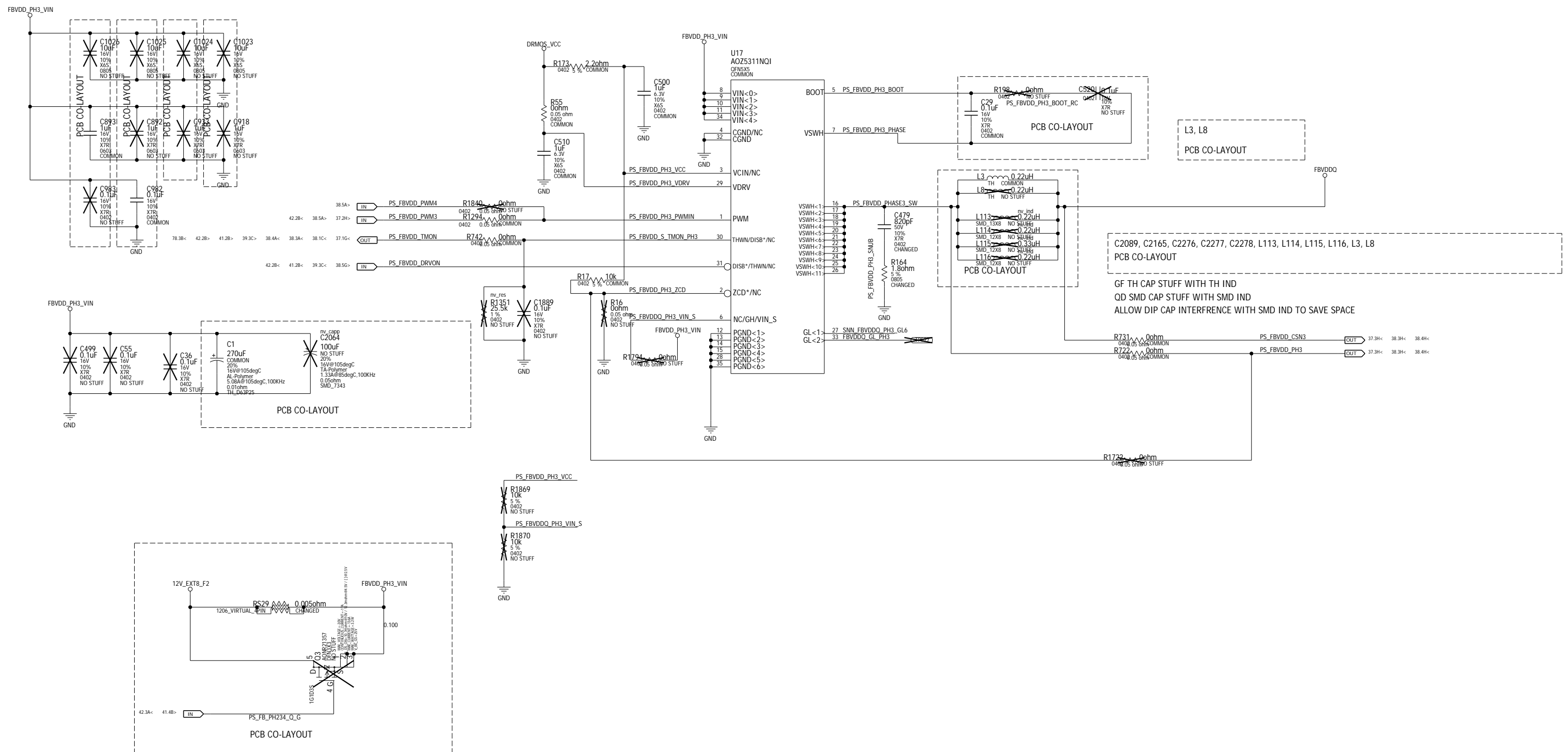
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PS: FBVDD PH3



FBVDD PH3 INPUT ANTI-BACKDRIVE

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: FBVDD PH3

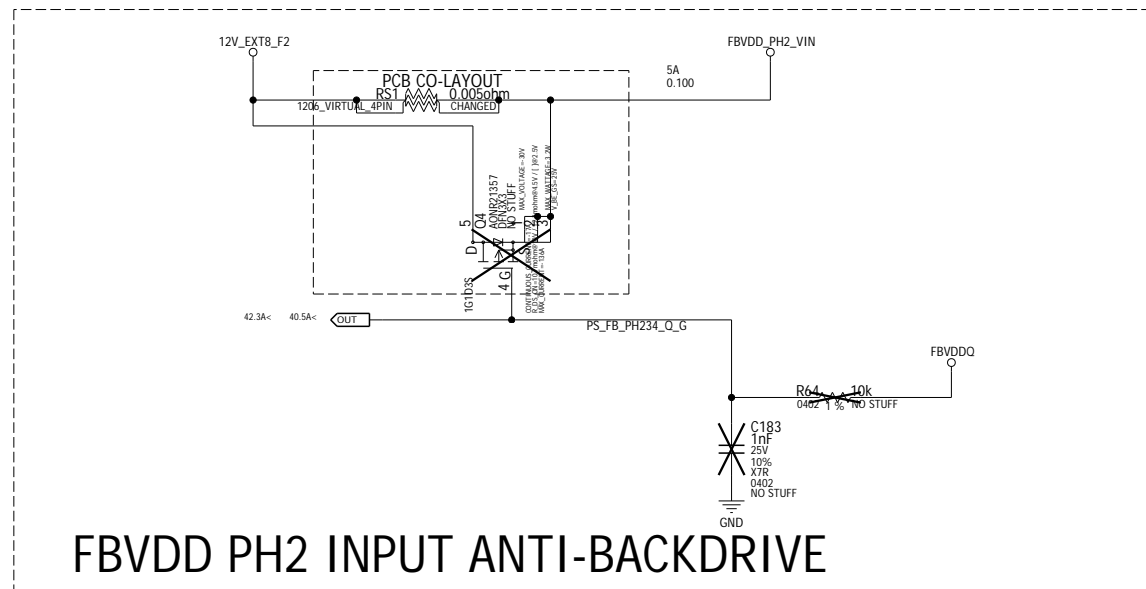
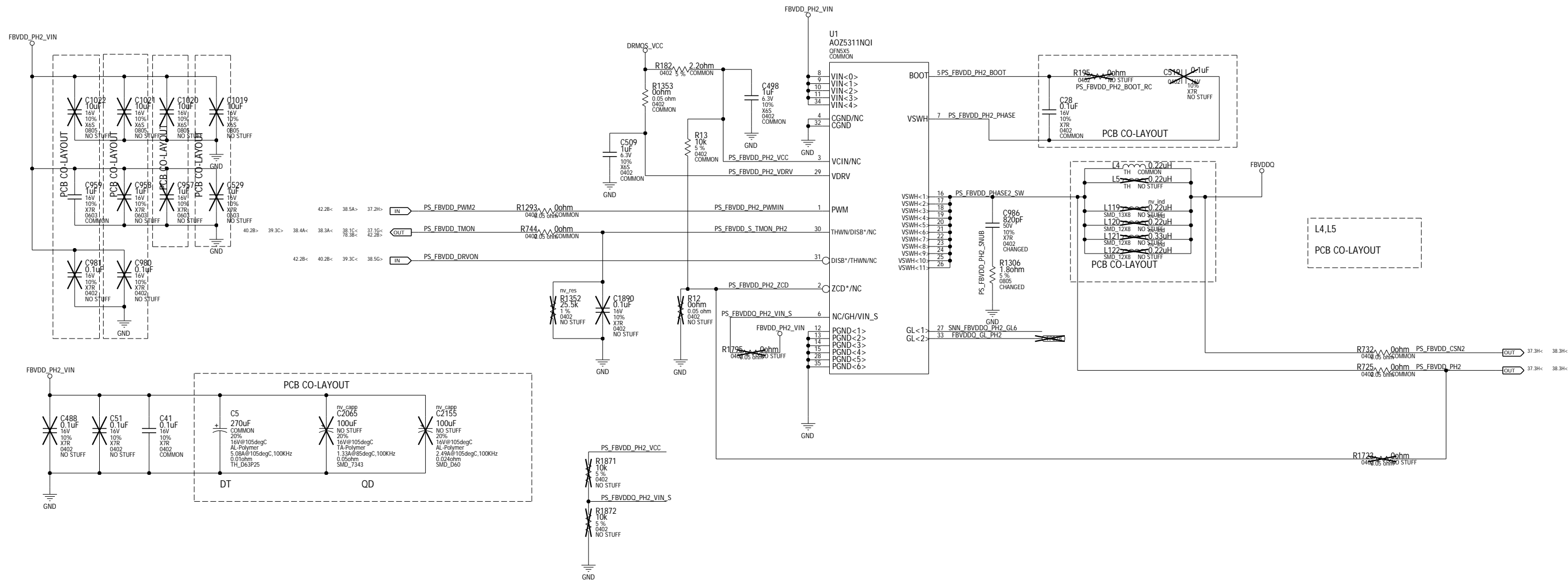
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PS: FBVDD PH2



FBVDD PH2 INPUT ANTI-BACKDRIVE

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: FBVDD PH2

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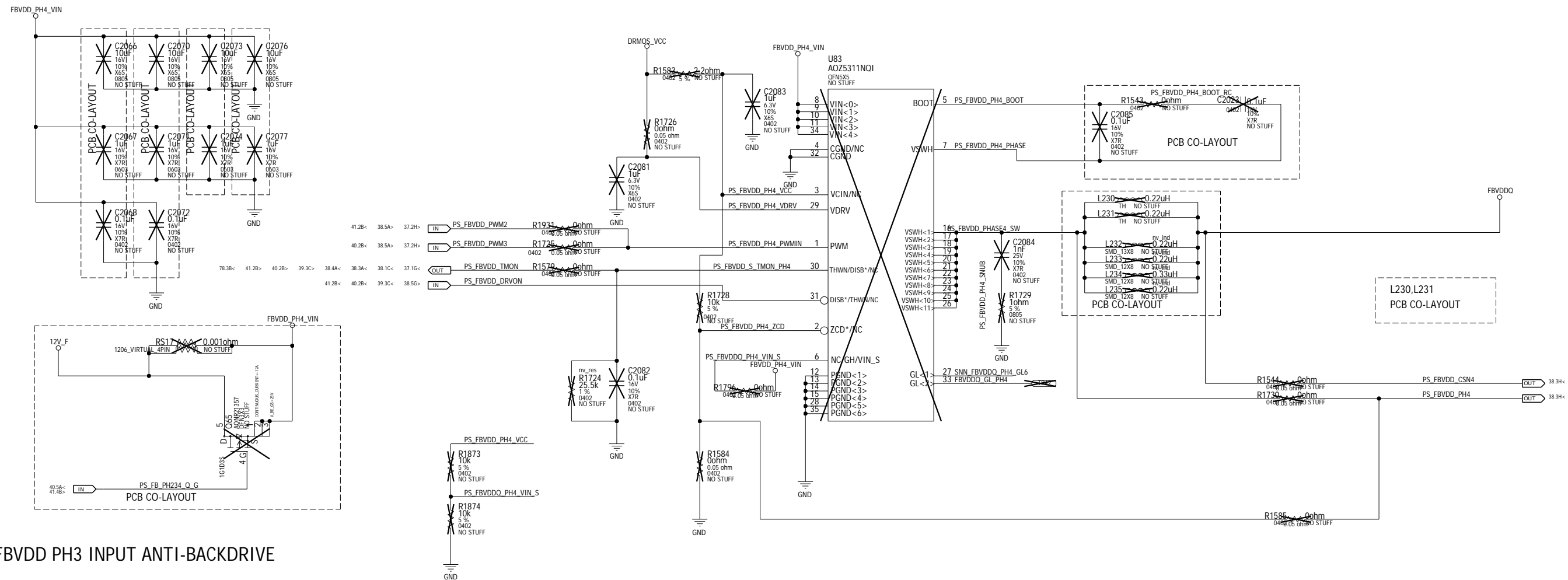


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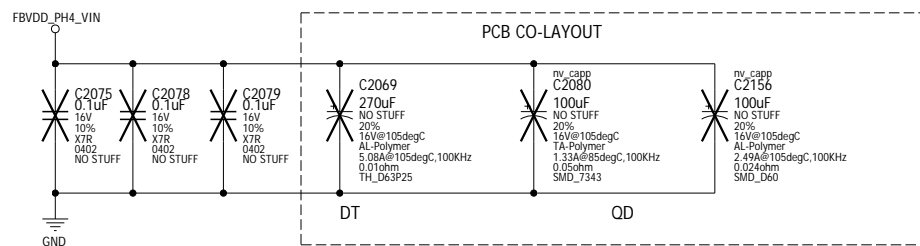
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PS: FBVDD PH4



FBVDD PH3 INPUT ANTI-BACKDRIVE



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PAGE DETAIL	PS: FBVDD PH4

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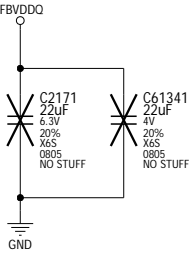
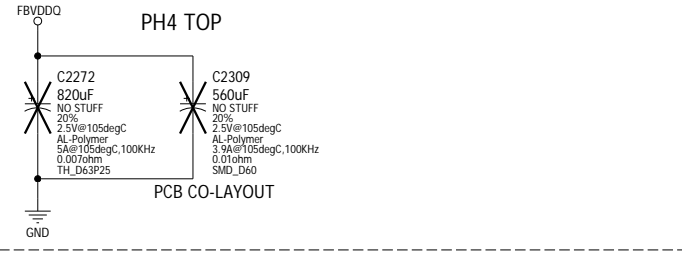
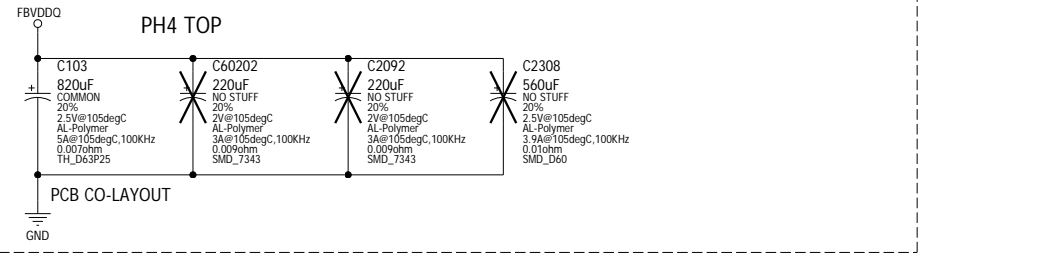
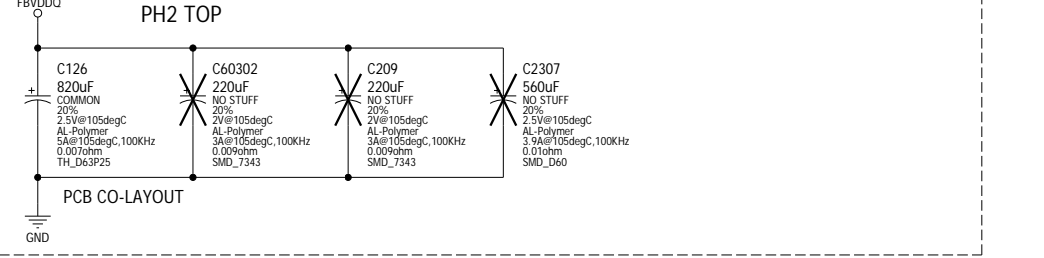
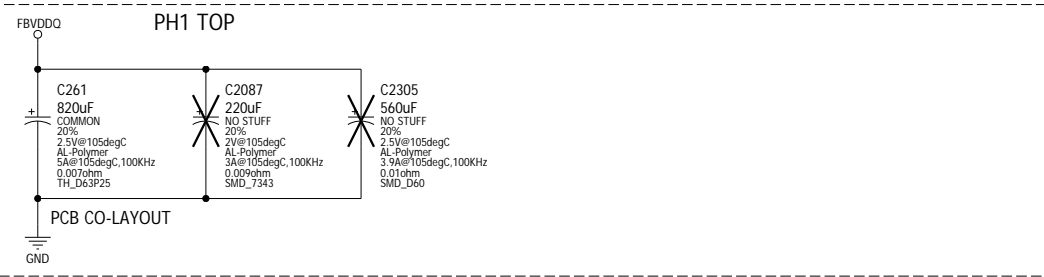


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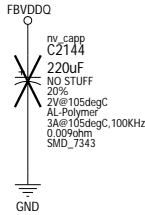
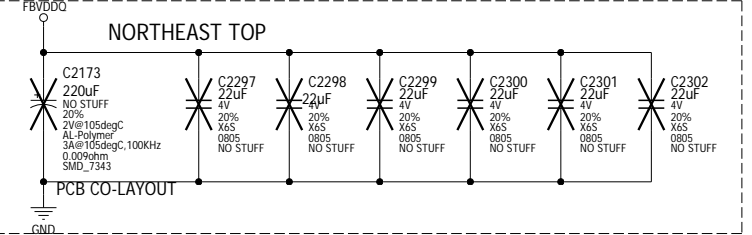
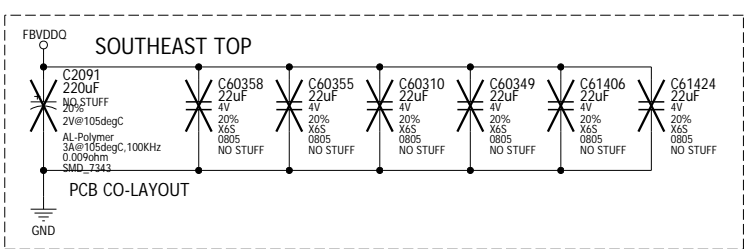
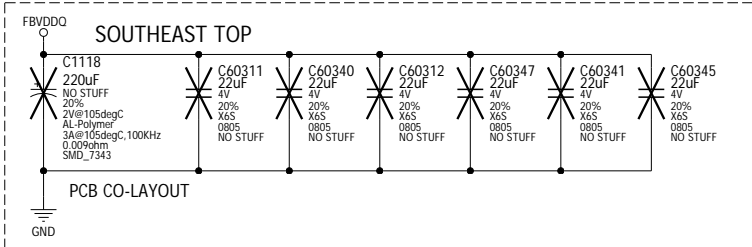
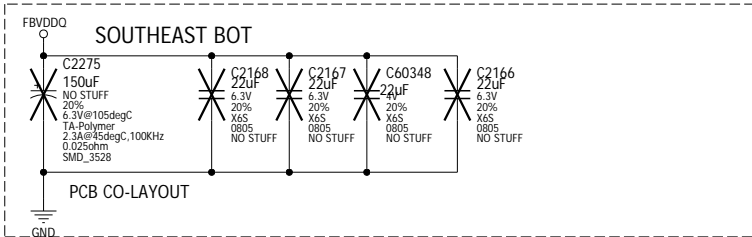
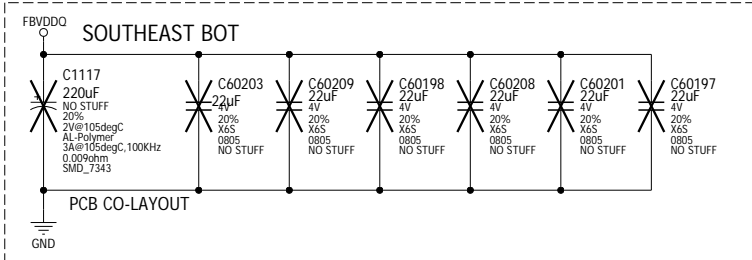
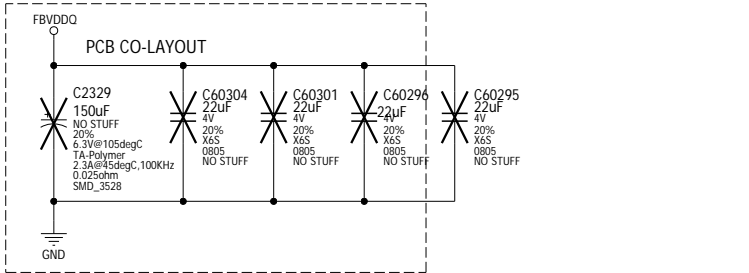
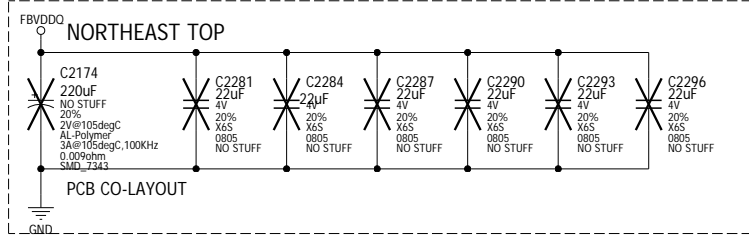
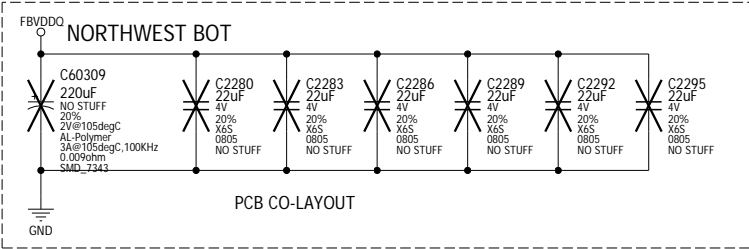
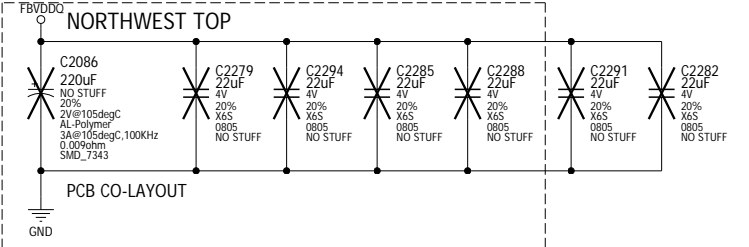
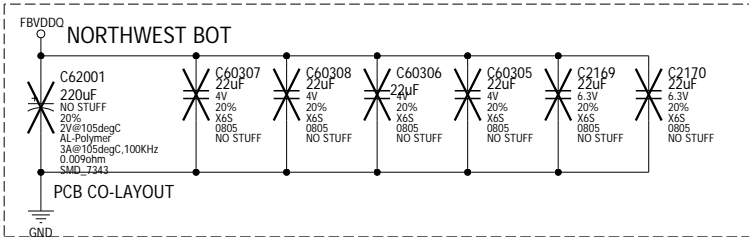
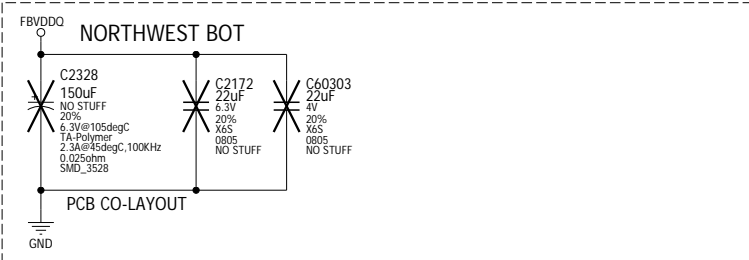
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PS: FBVDD OUTPUT CAP

3x 820uF TH FBVDD OUTPUT BULK CAPS

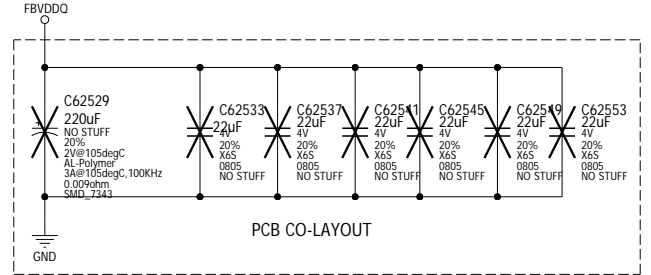
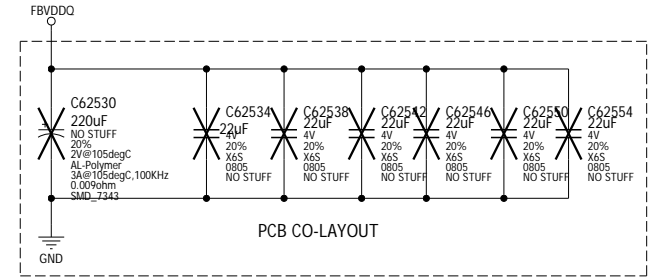
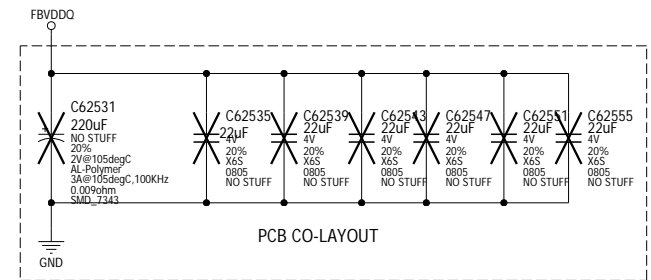
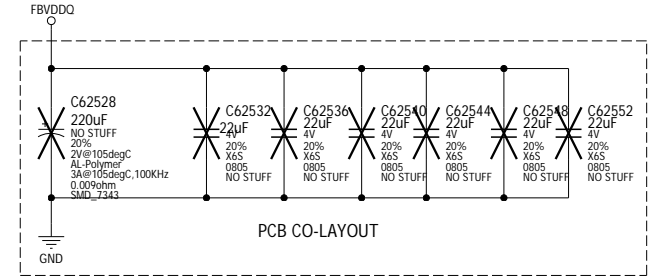
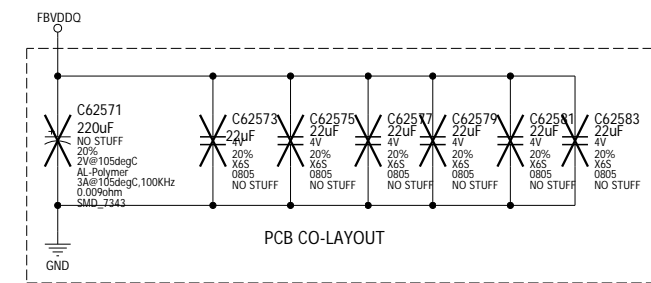
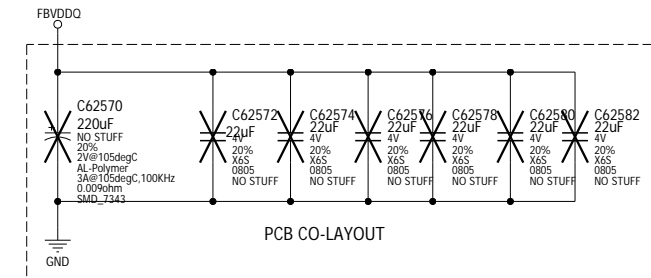
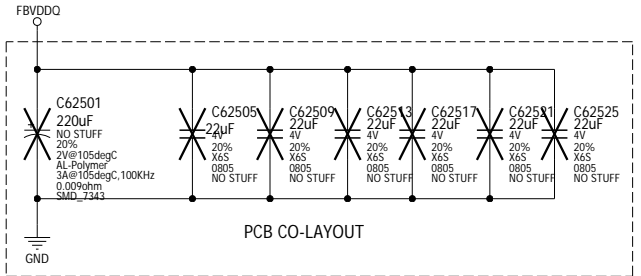
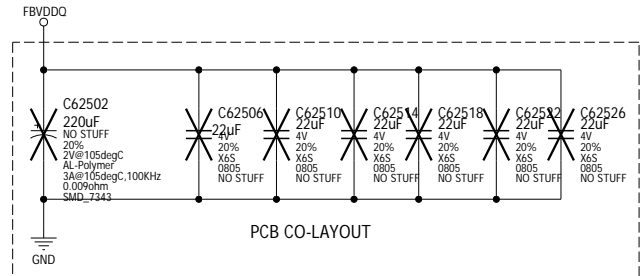
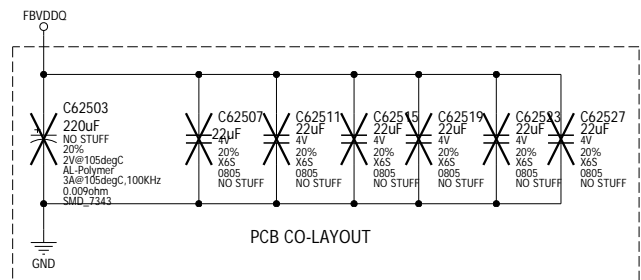
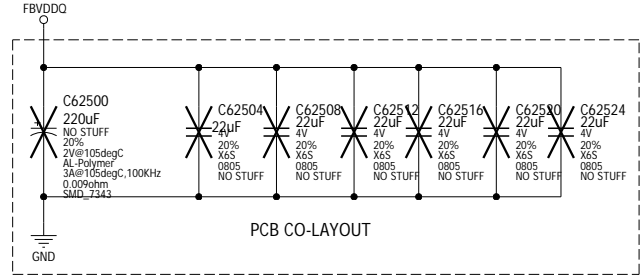
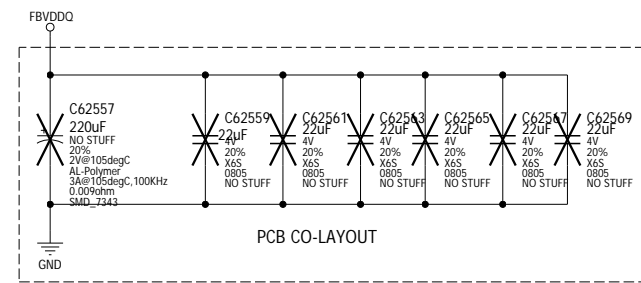
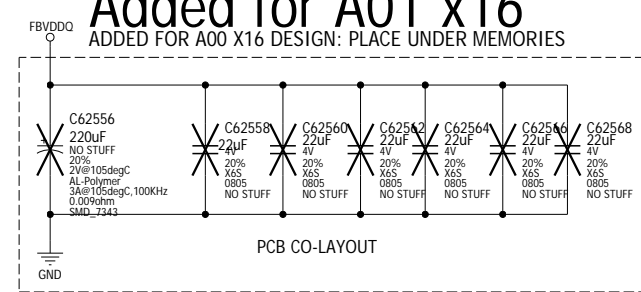


CLOSE TO FB PH3 OUTPUT STUFF



Added for A01 x16

ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES



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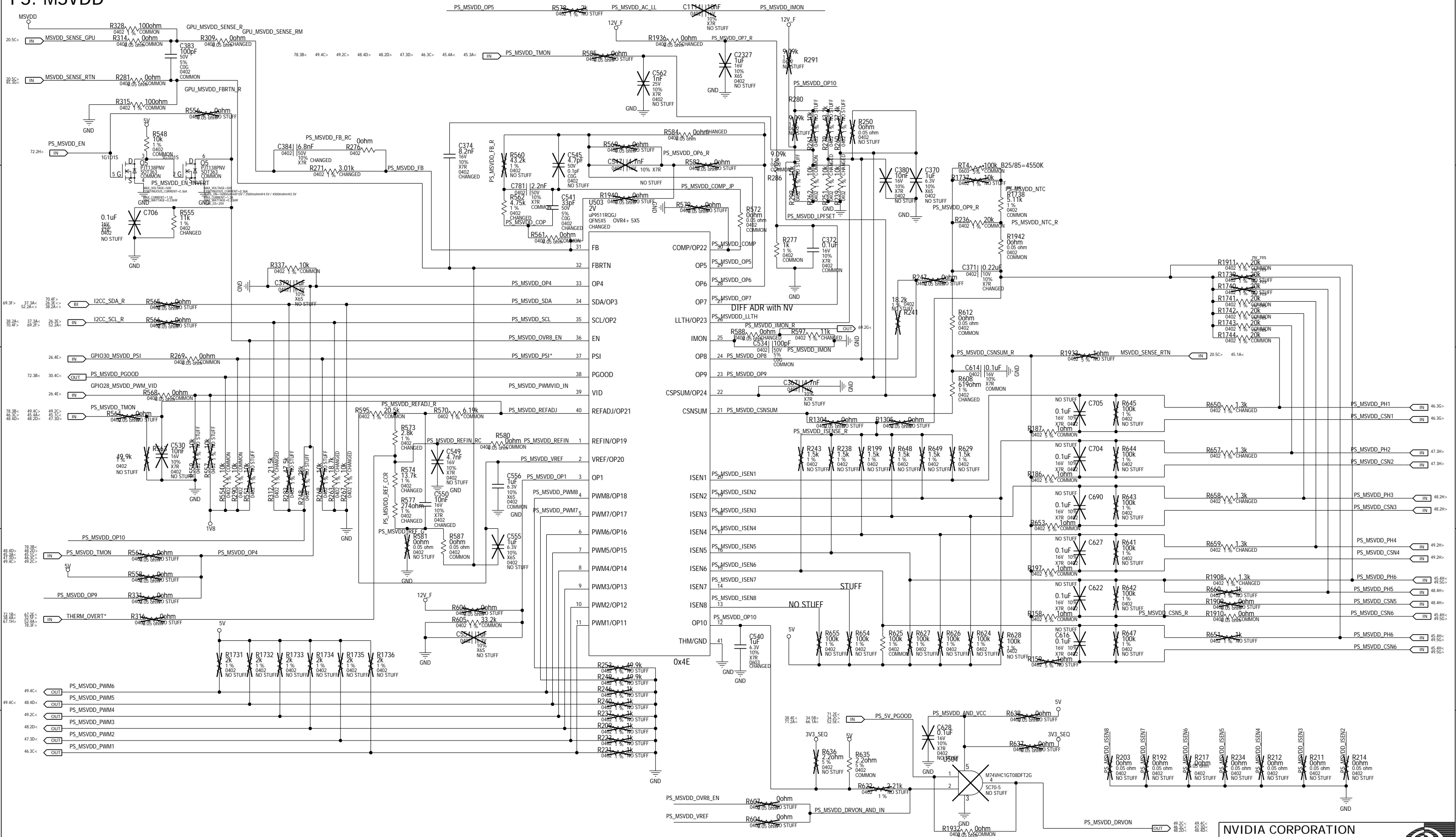
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PAGE DETAIL	PS: FBVDD_OUTPUT_CAP_NEAR_MEMORY

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PS: MSVDD



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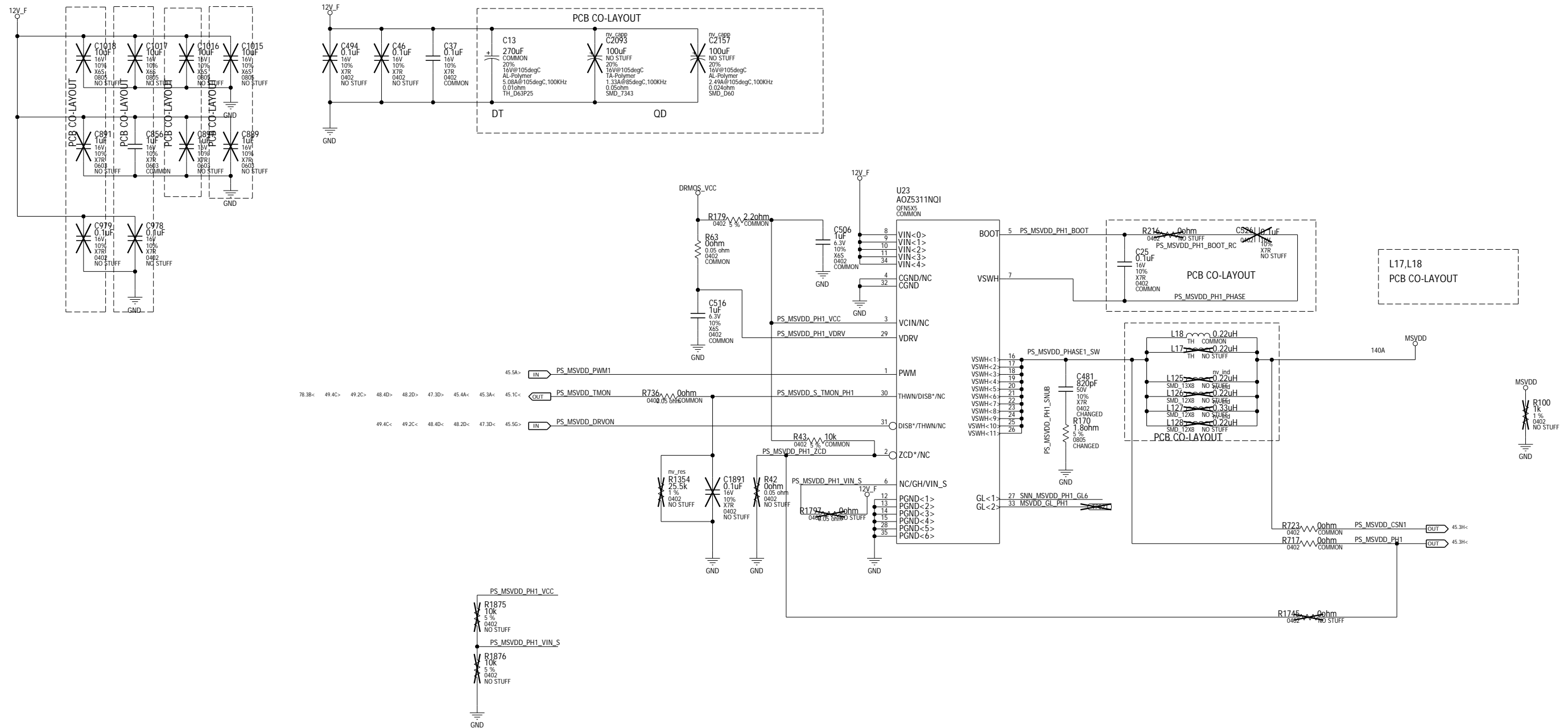
PAGE

DATE

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15-JUN-2020

PS: MSVDD Phase 1



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PAGE DETAIL	PS: MSVDD PH1

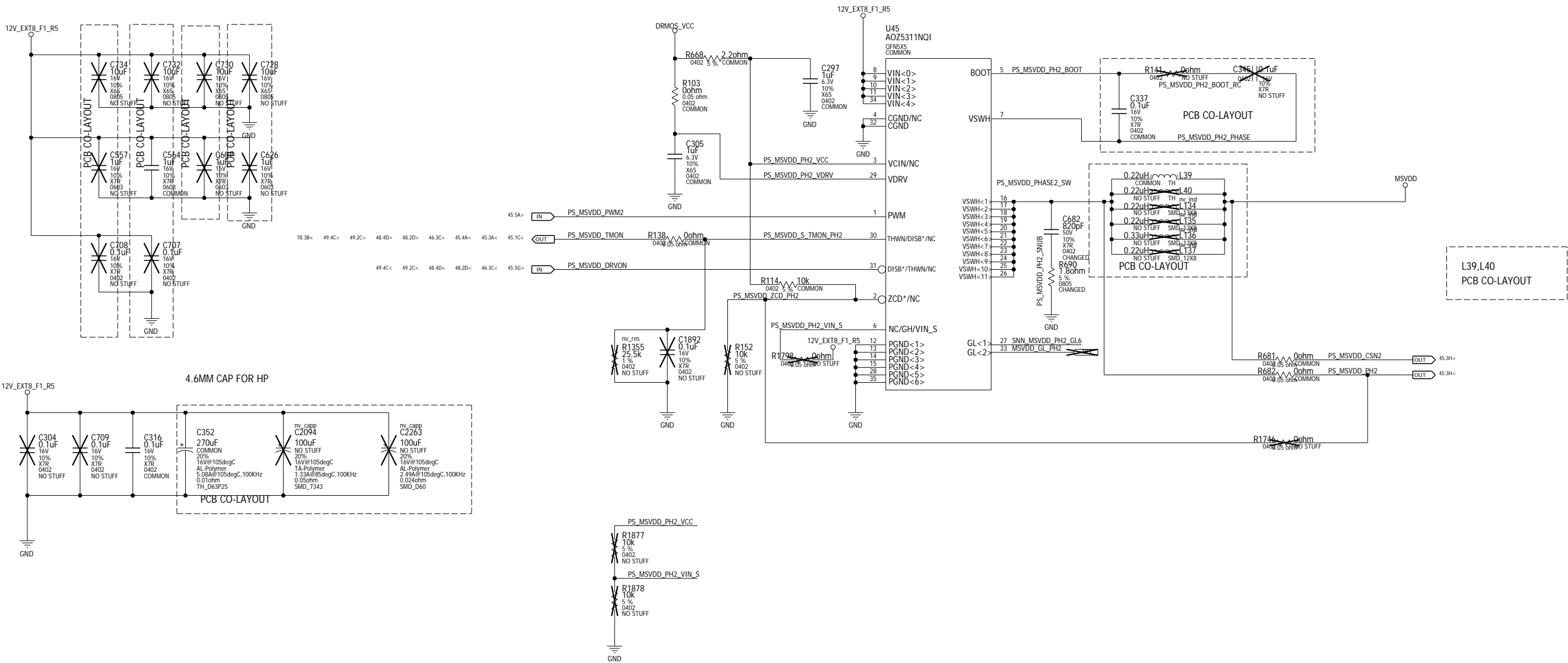
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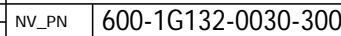
NV_PN	600-1G132-0030-300		
PCB REV	PG132-A02	PAGE	46 OF 79
BOM REV	C	DATE	15-JUN-2020

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PS: MSVDD PH 2

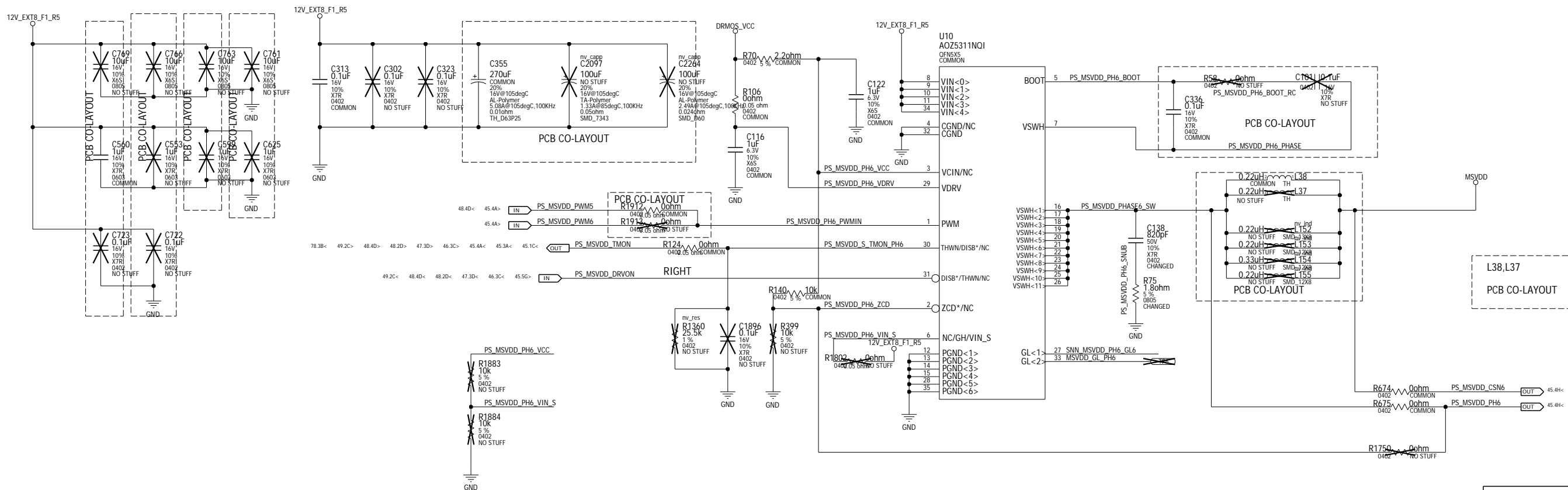
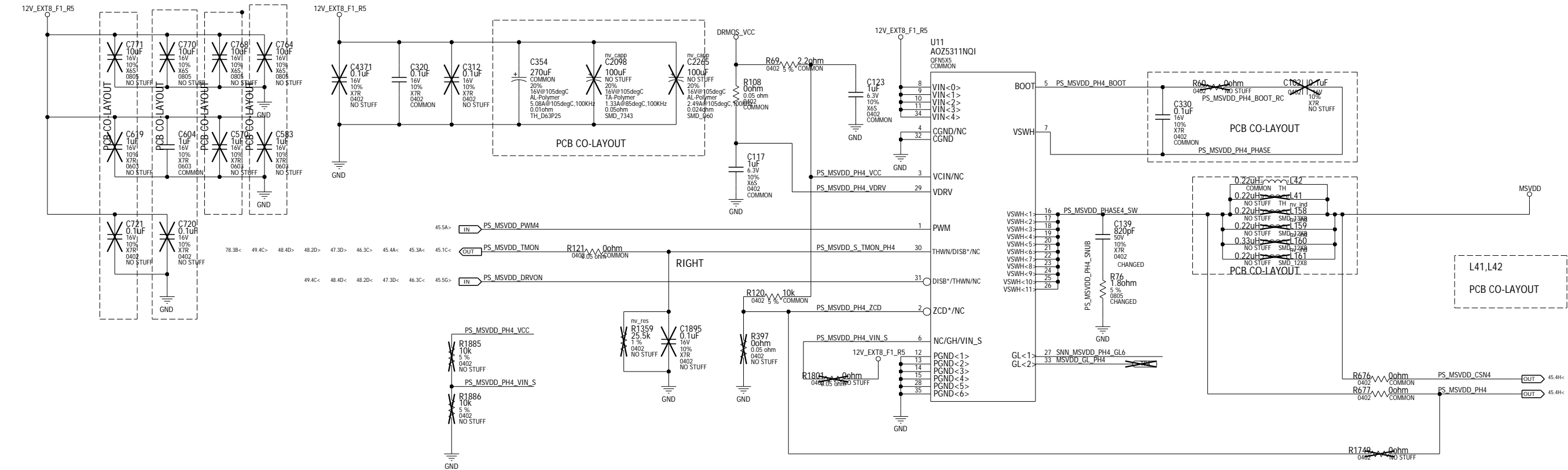


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PS: MSVDD PH 4,6



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: MSVDD PH4 and PH6

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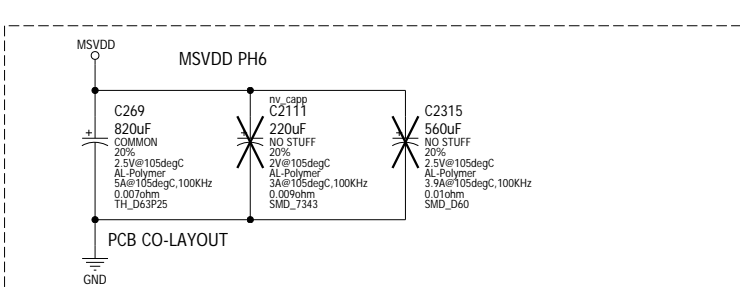
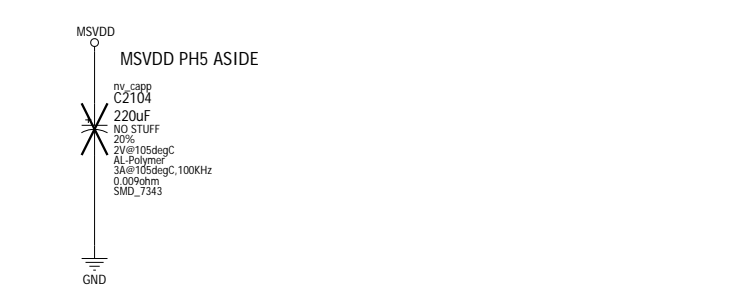
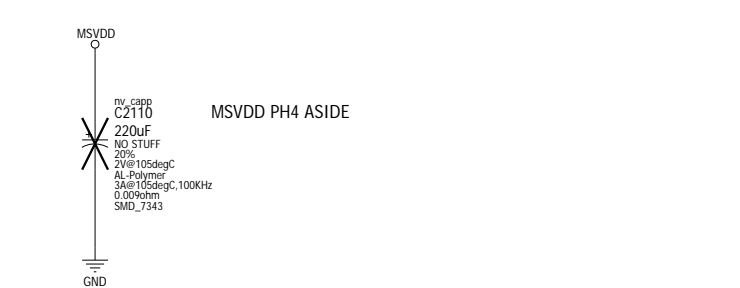
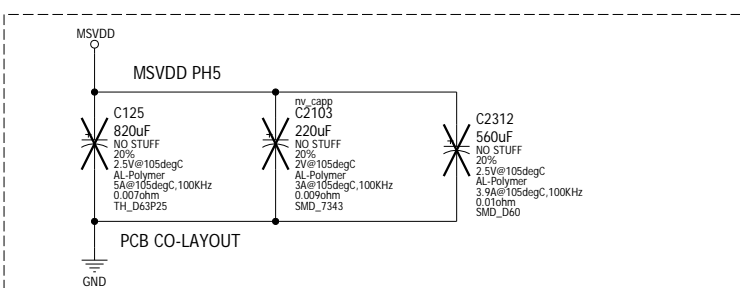
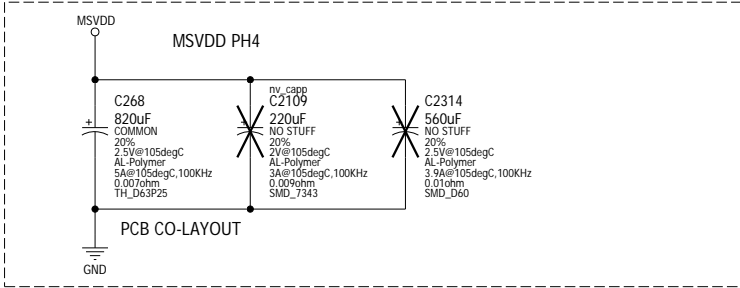
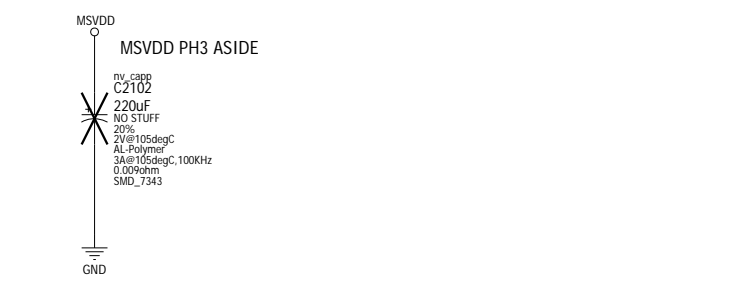
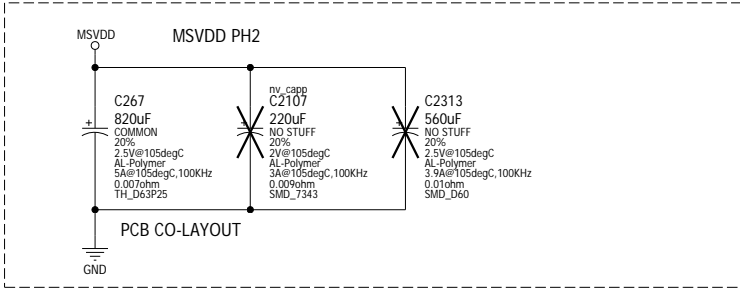
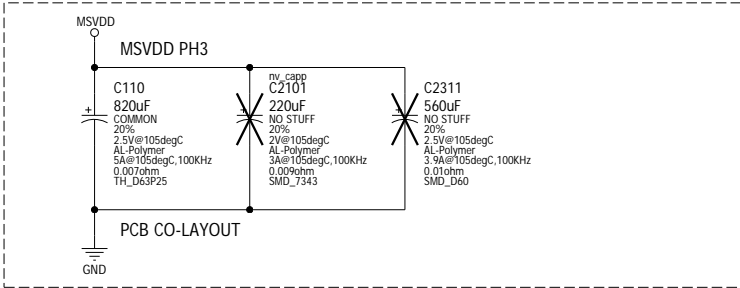
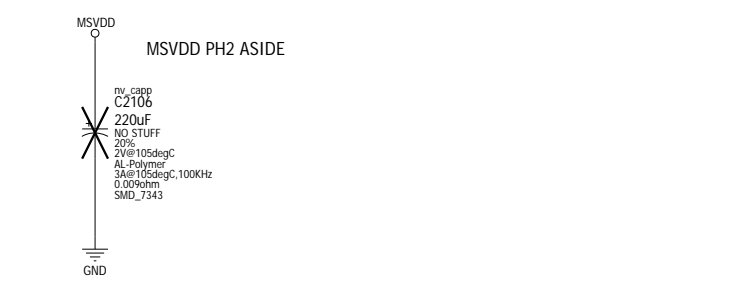
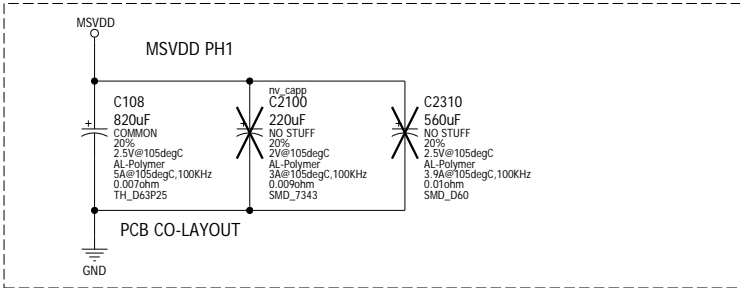
NV_PN	600-1G132-0030-300
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DATE	TIME	TO GO	TO GO

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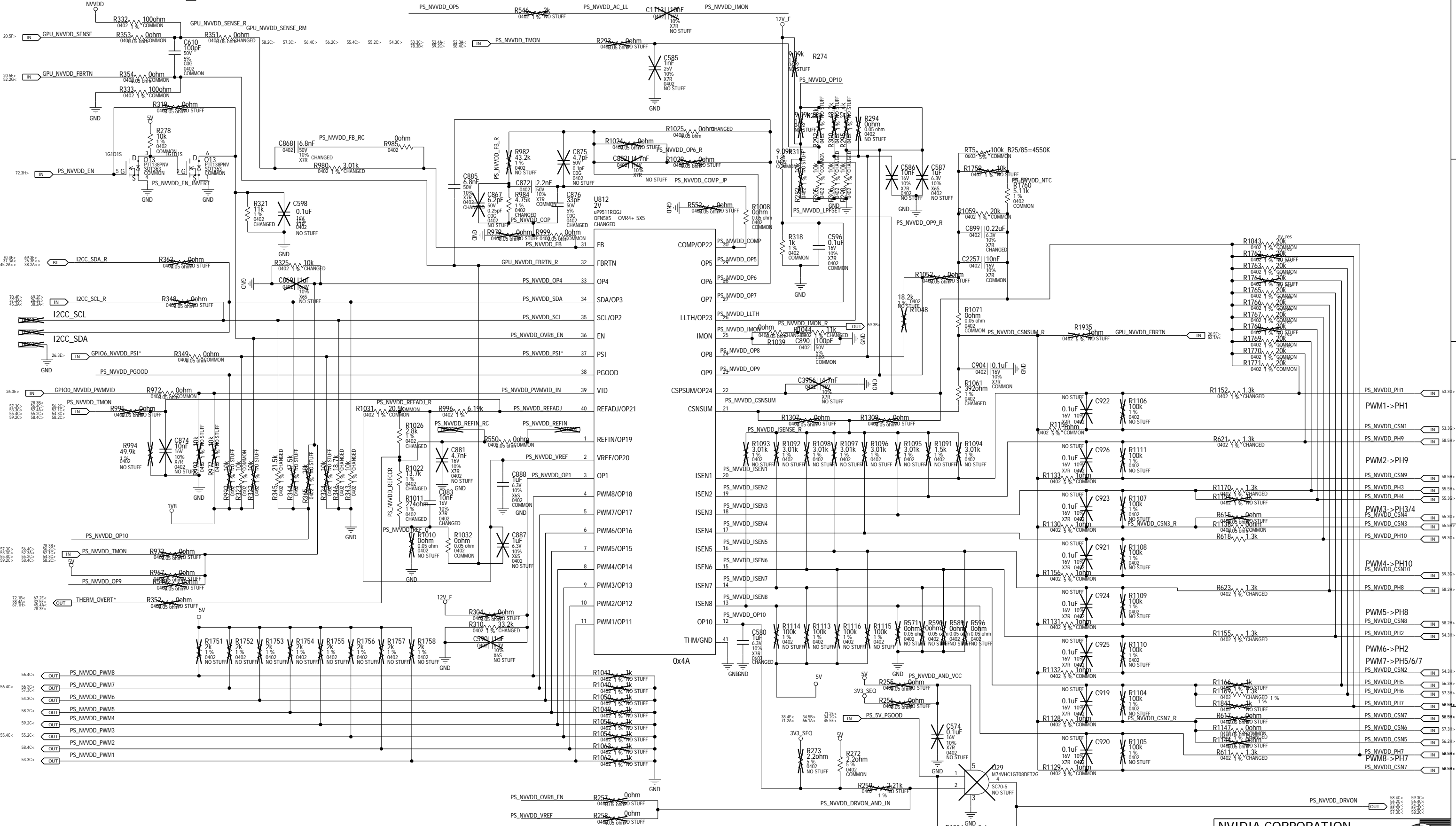
PS:MSVDD OUTPUT CAP (TOP)



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PS: NVVDD Controller_OVR8



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVDD Controller_OVR8

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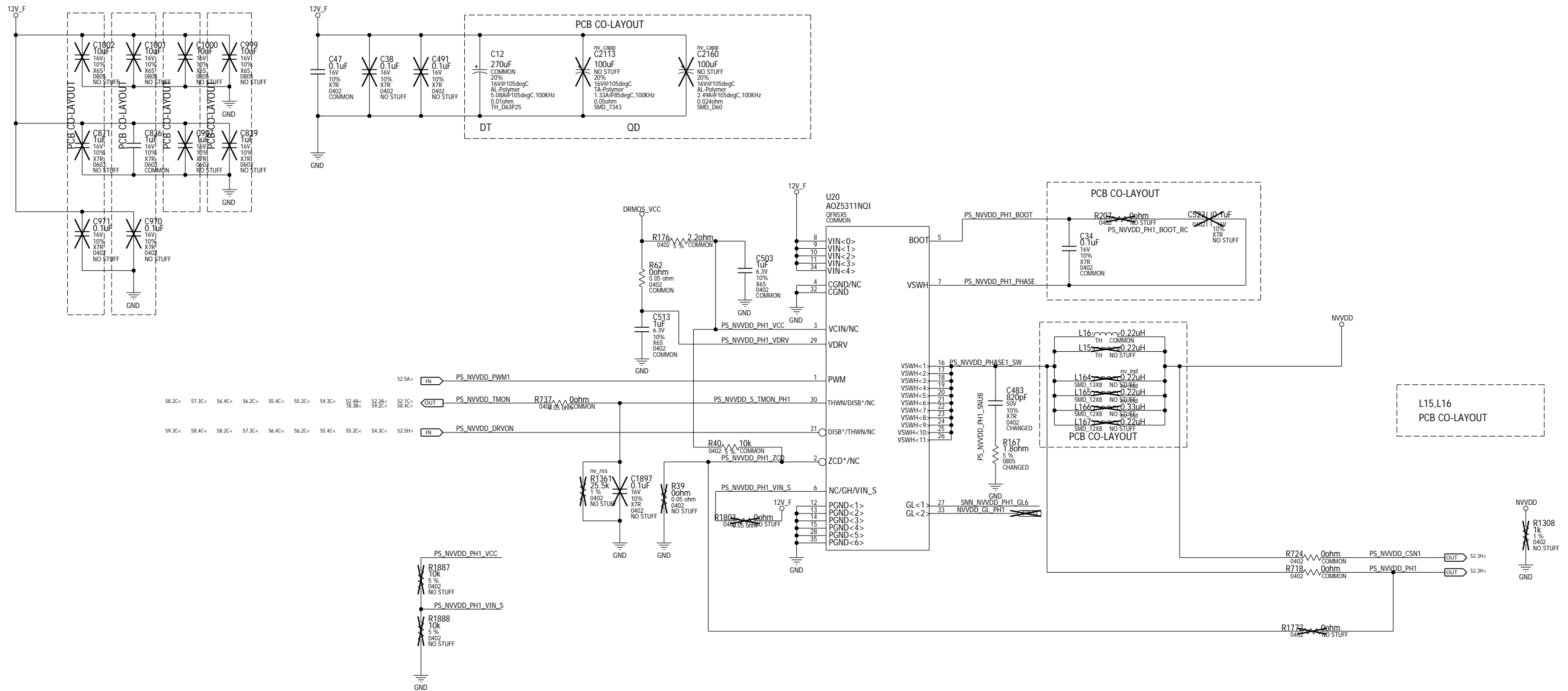
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BOM REV	C	DATE	15-JUN-2020

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PS: NVVDD Phase 1



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH1 (PWM1)

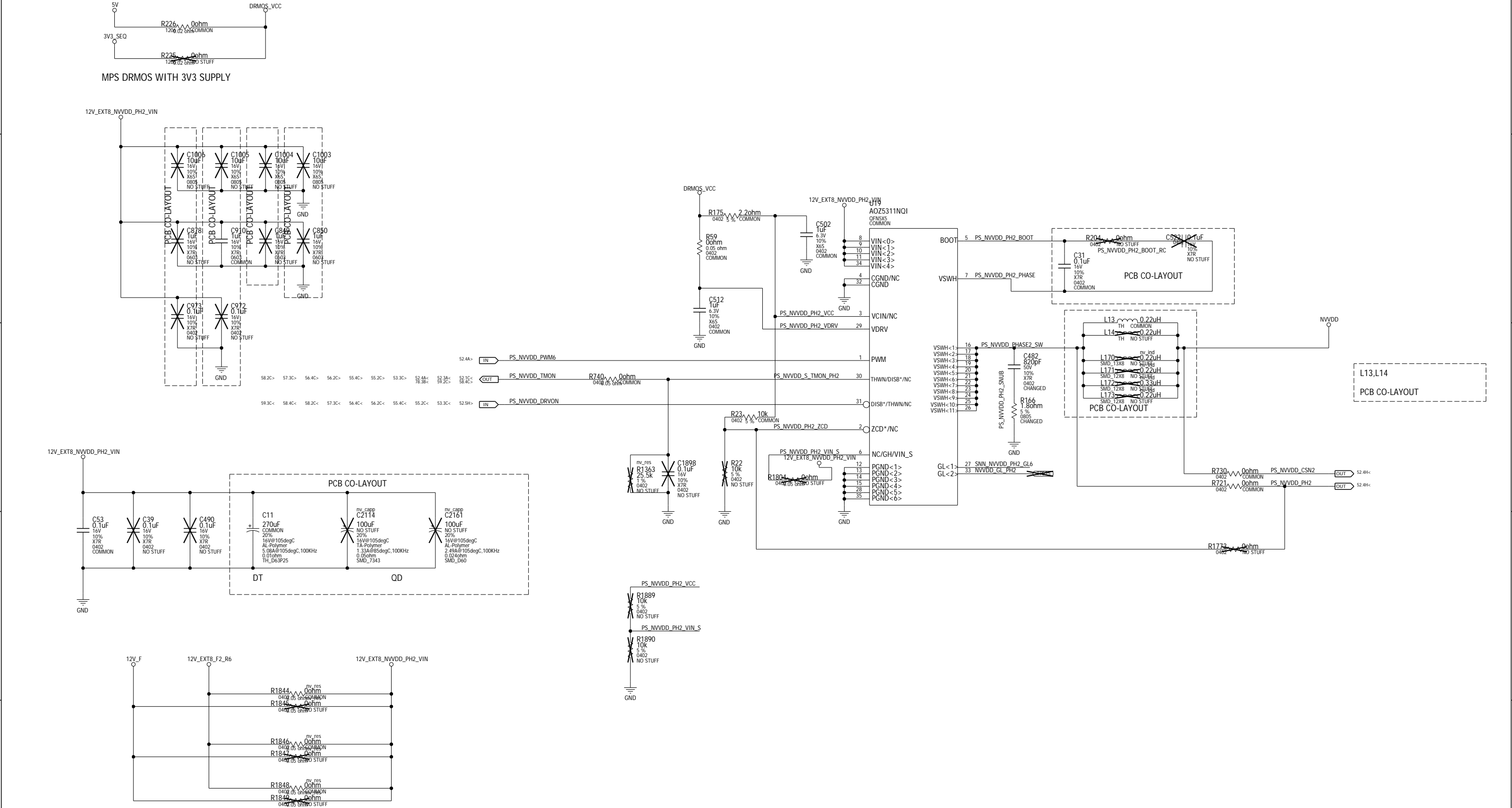
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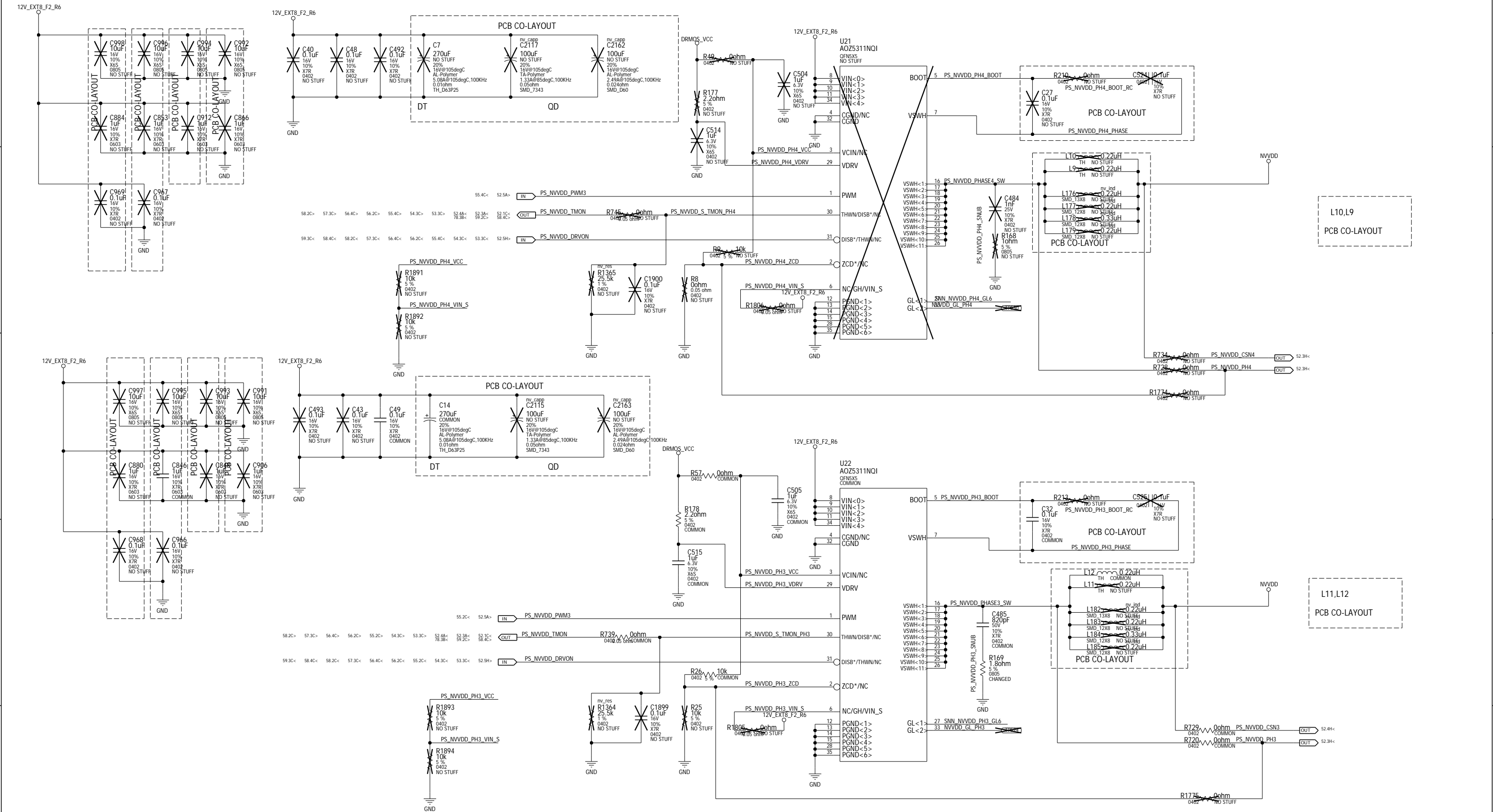
NV_PN	600-1G132-0030-300		
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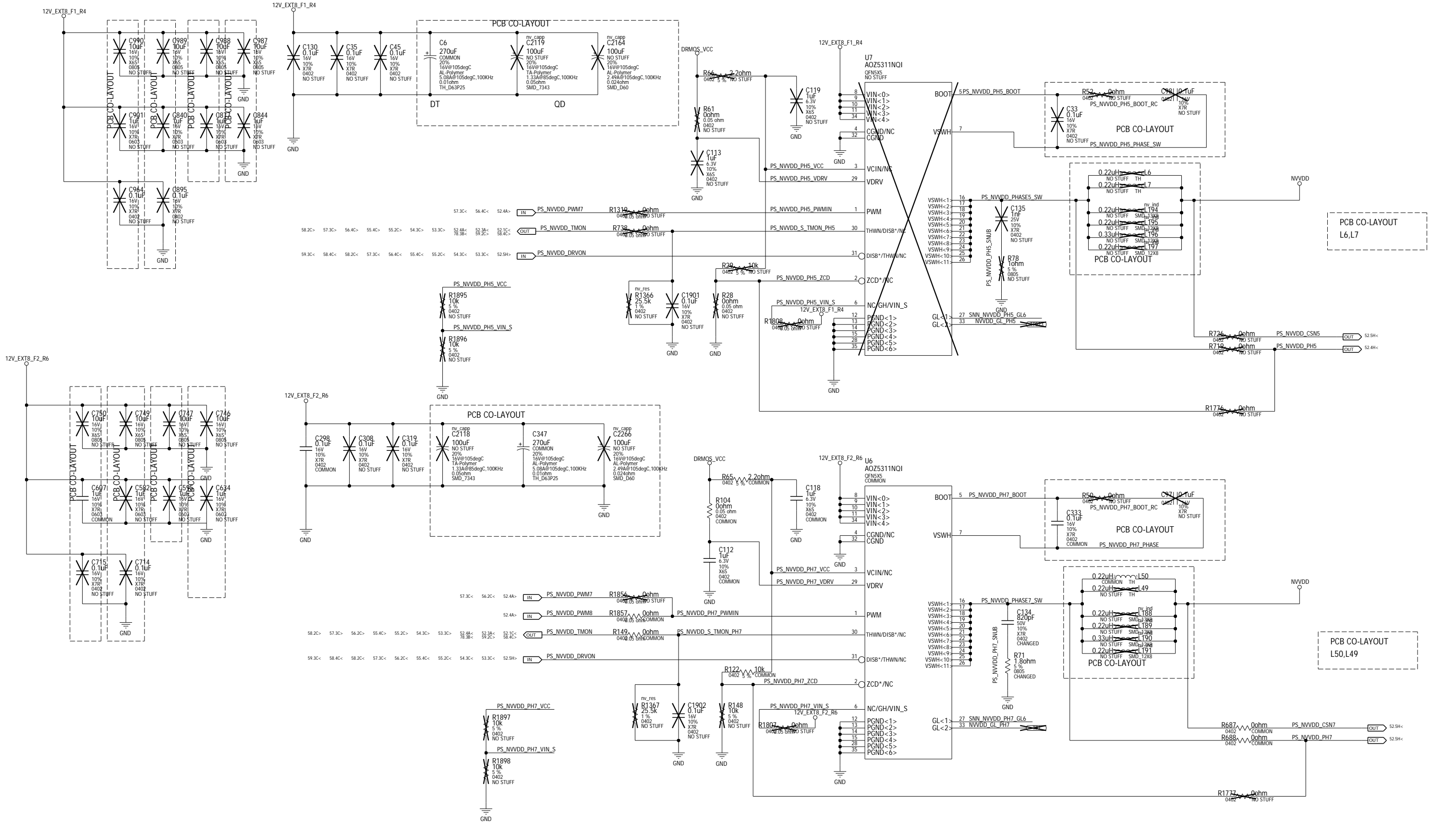
PS: NVVDD Phase 2



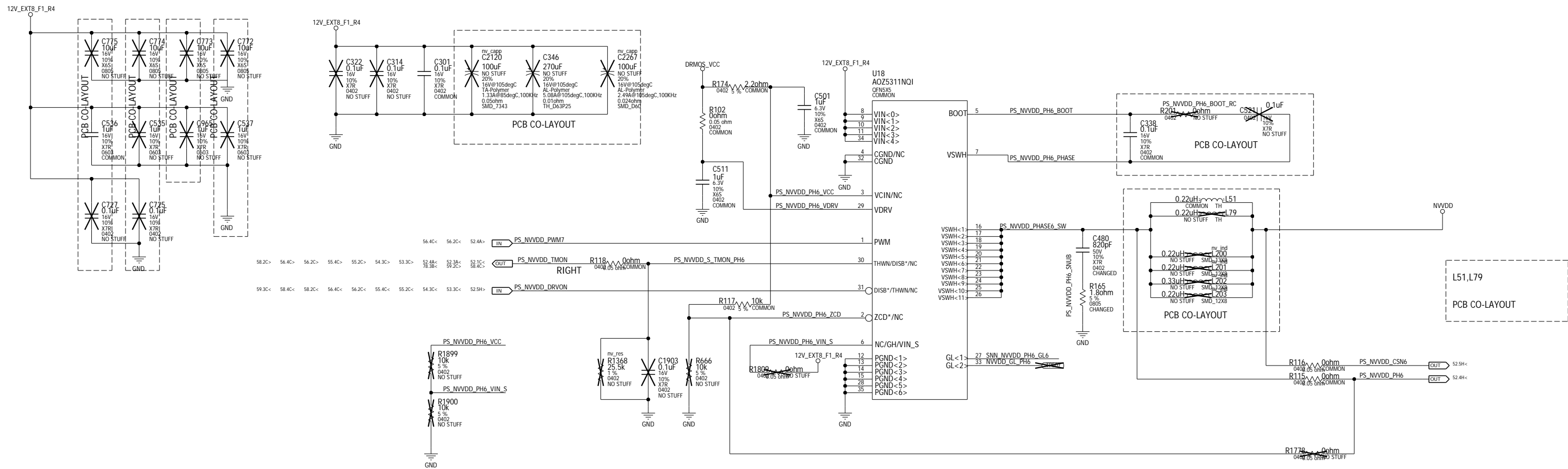
PS: NVVDD Phase 3 (PWM6), PHASE 4(PWM2)



PS: NVVDD PH 5(PWM2), PH7(PWM3)



PS: NVVDD Phase 6(PWM7)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH6 (PWM7)

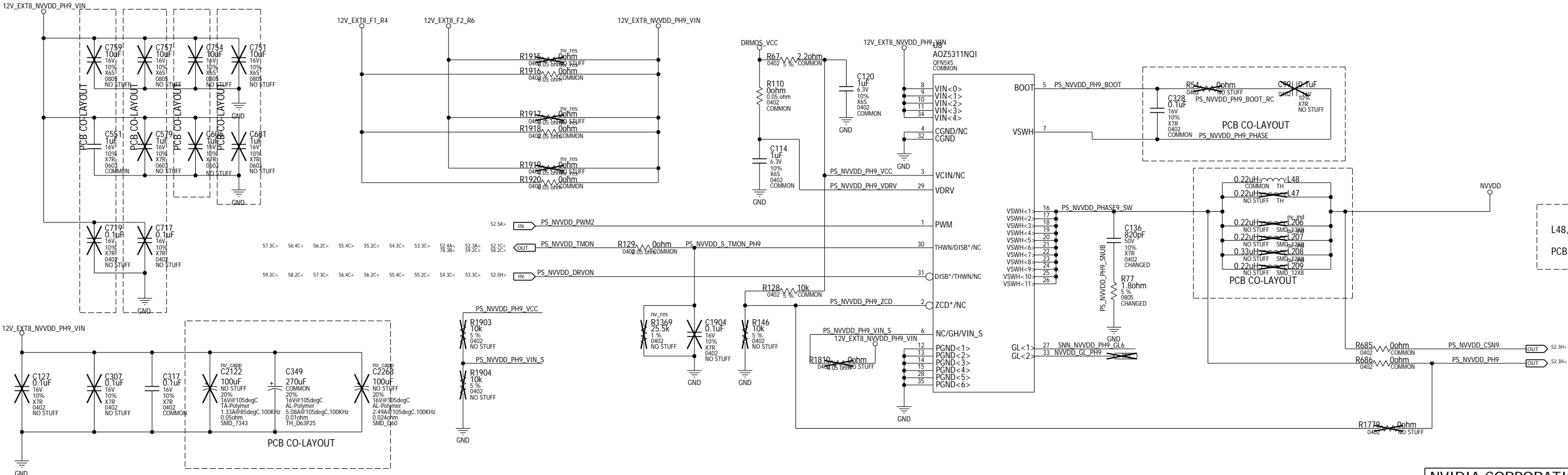
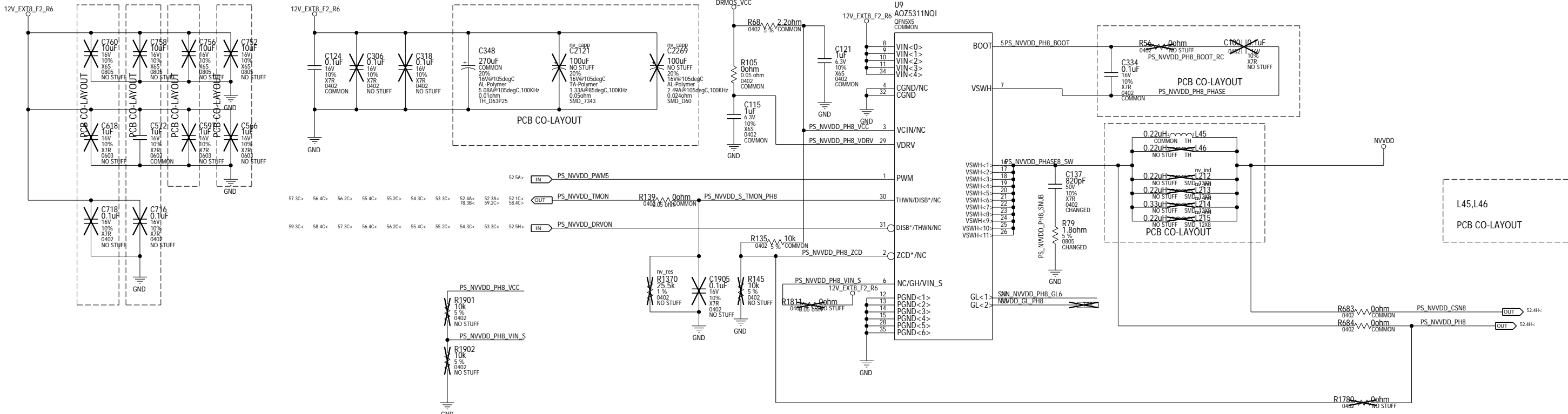
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PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH8(PWM5) and PH9(PWM2)

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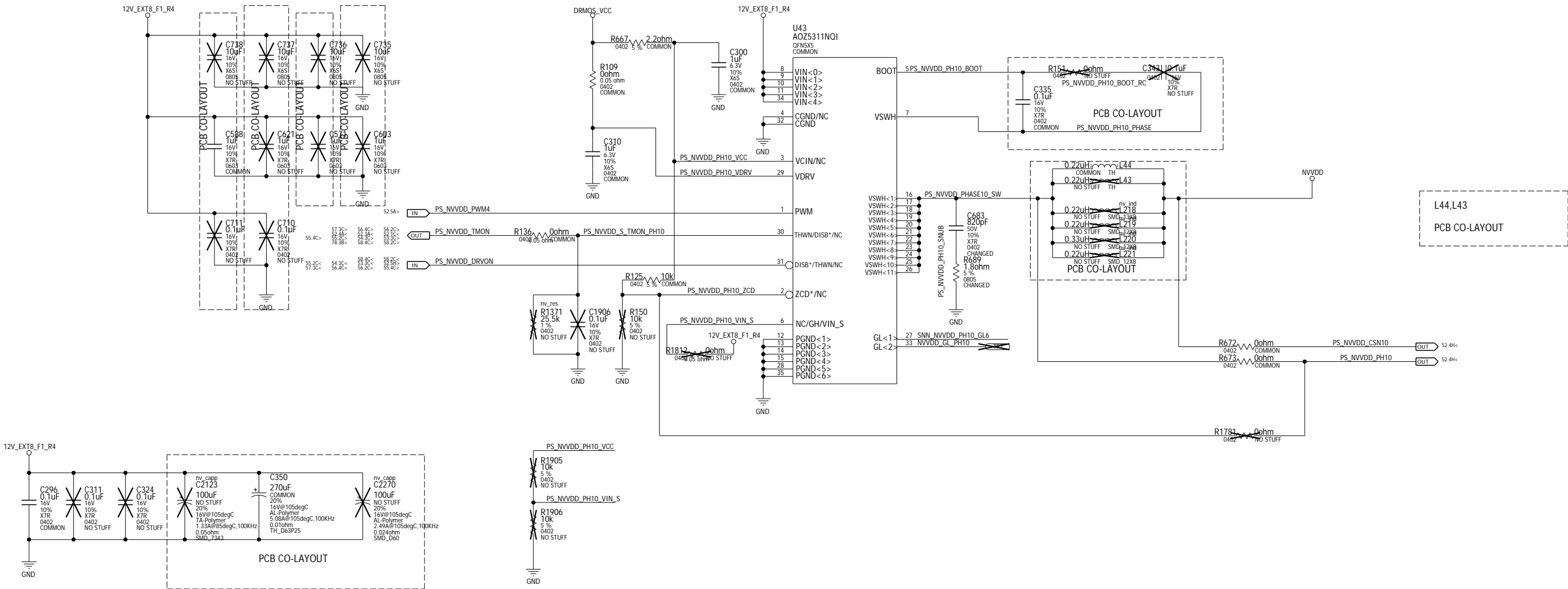
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PCB REV	PG132-A02	F
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	15 JUN 2022

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PS: NVVDD Phase 10 (PWM8)



A	B	C	D	E	F	G	H
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PCB CO-LAYOUT
C131, C132, C133, C140, C141, C142, C2106, C2107, C2133, C2134, C2135, C2137, C264, C265, C266, C267, C61, C64, C65, C66, C67, C68, C69, C77, C80, C83, C88

PCB CO-LAYOUT
C103, C105, C106, C107, C108, C110, C1208, C125, C1254, C1256, C1267, C128, C144, C145, C146, C151, C152, C153, C154, C159, C160, C161, C162, C170, C173, C2092, C2100, C2101, C2102, C2103, C2104, C2138, C2139, C2140, C2141, C2142, C2143, C2144, C2272, C230, C231, C232, C233, C243, C245, C246, C248, C253, C254, C255, C256, C270, C274, C275, C276, C283, C289, C290, C291, C60202, C62004, C62005

C163, C164, C166, C167, C2087, C2105, C2109, C2110, C2111, C224, C225, C261, C268, C269, C60354, C61428, C62, C63, C89, C91, C96

PCB CO-LAYOUT

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PAGE DETAIL	Colayout_Notes

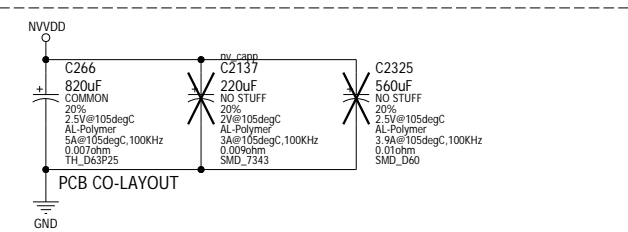
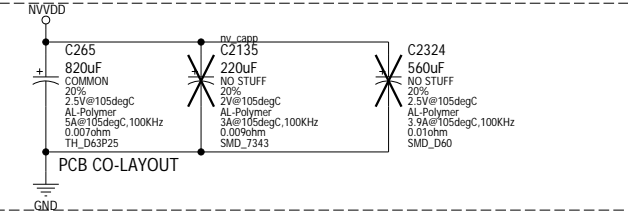
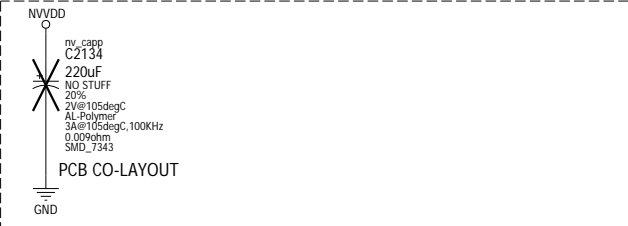
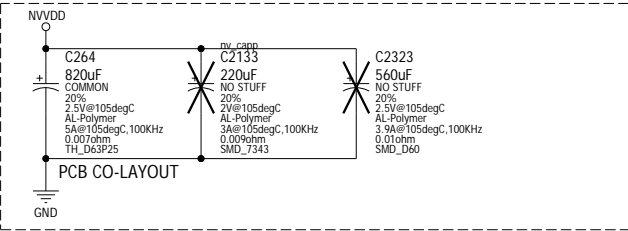
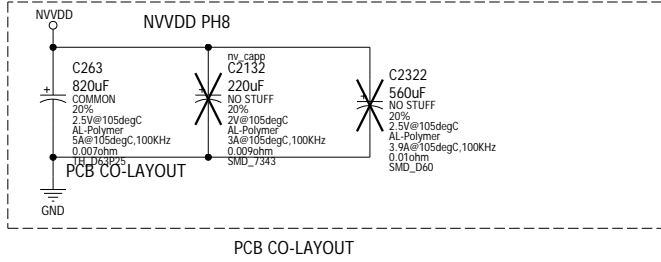
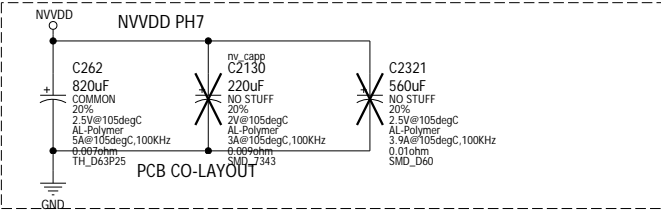
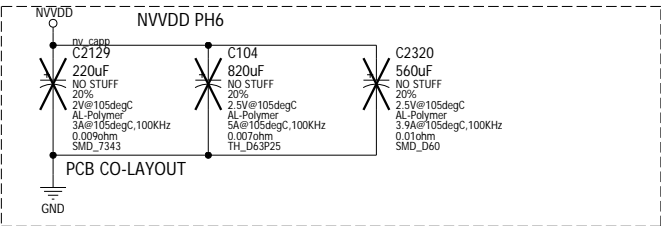
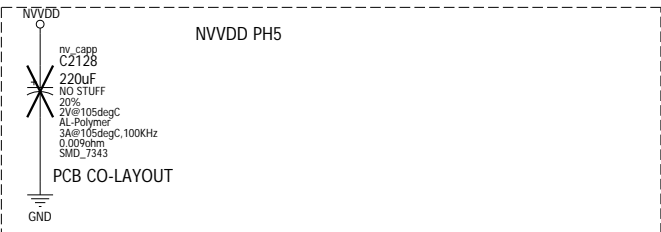
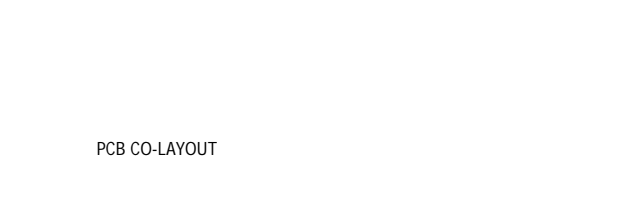
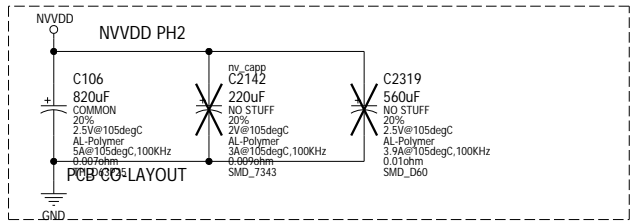
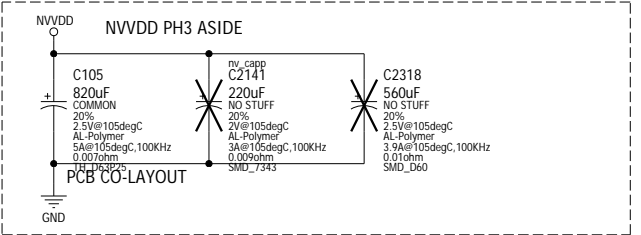
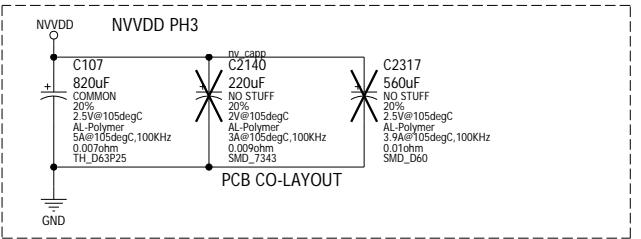
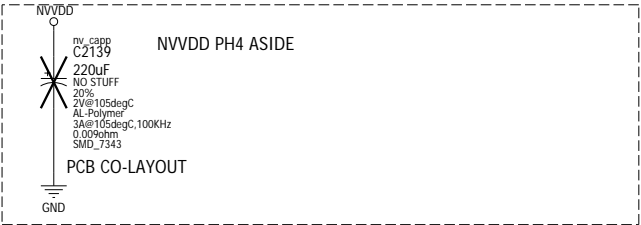
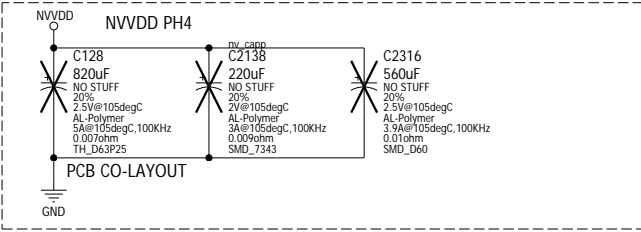
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BOM REV	C		

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PS: NVVDD OUTPUT CAP(TOP)

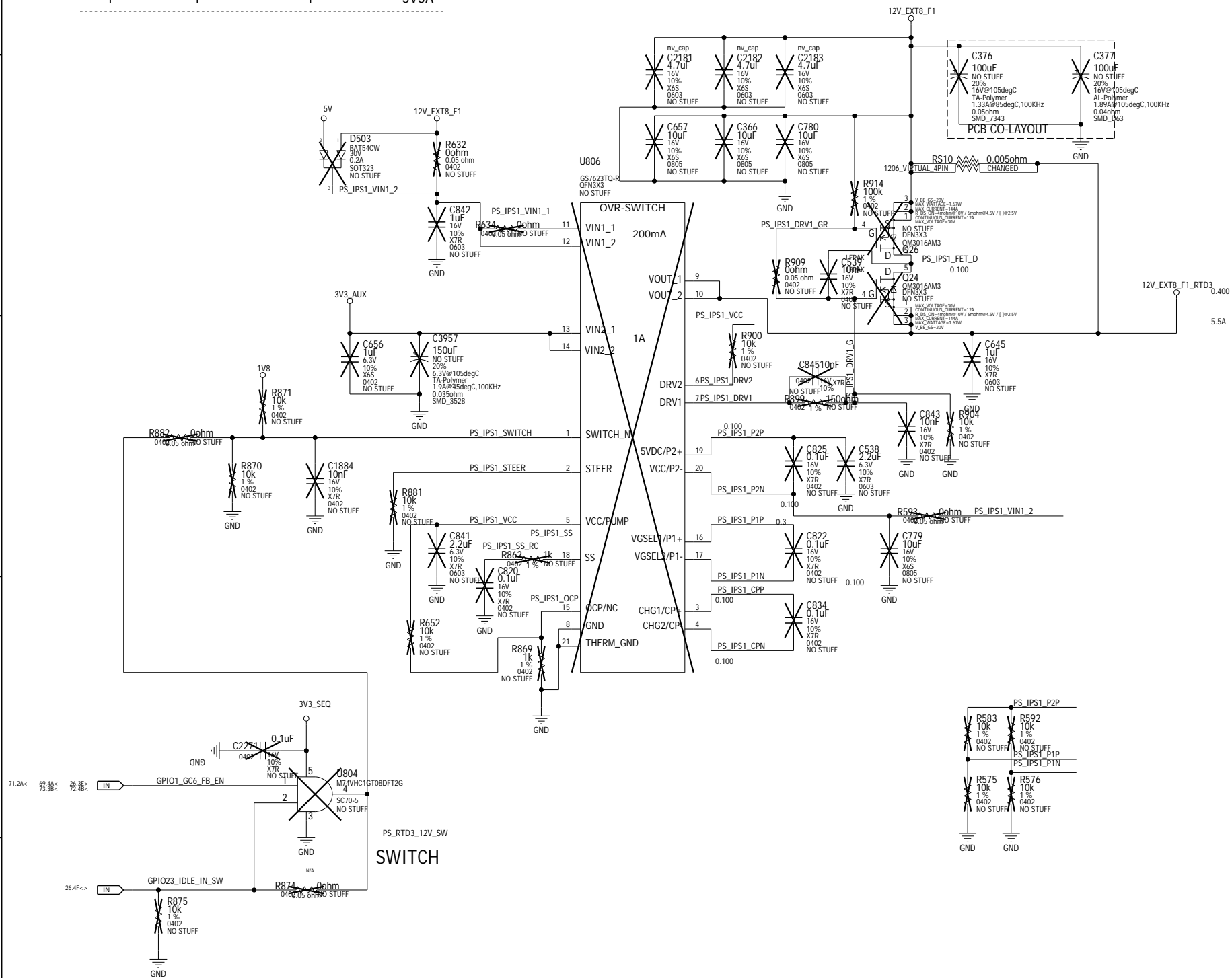


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PS: INPUT SWITCH RTD3

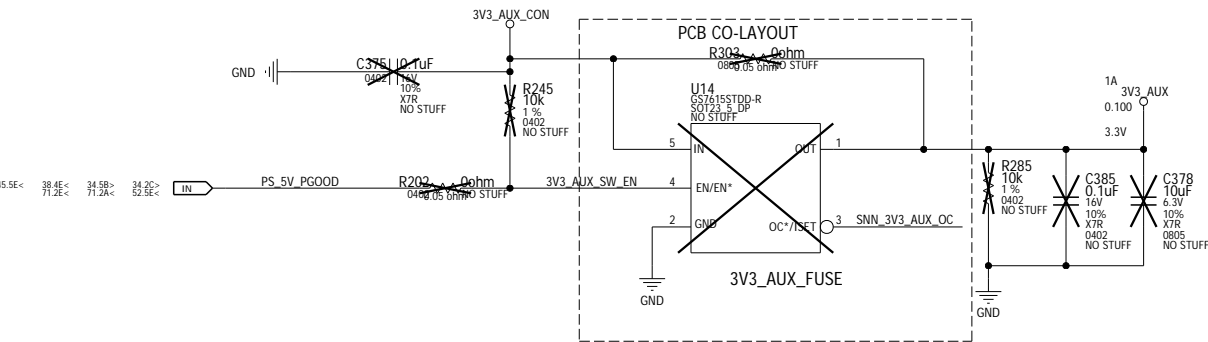
AND GATE LOGIC FOR P-BOARD

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0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

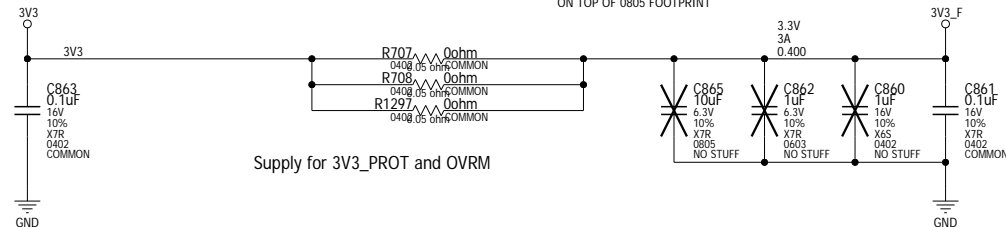


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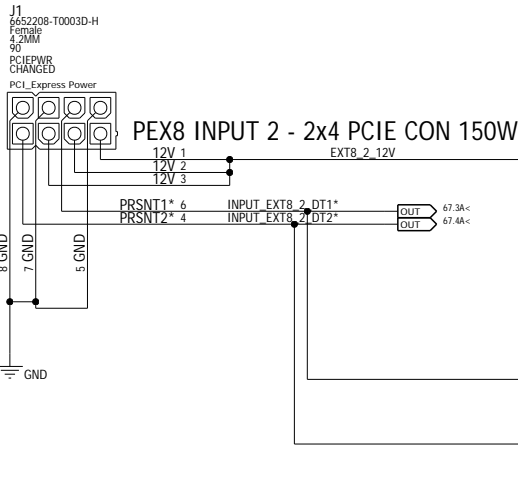
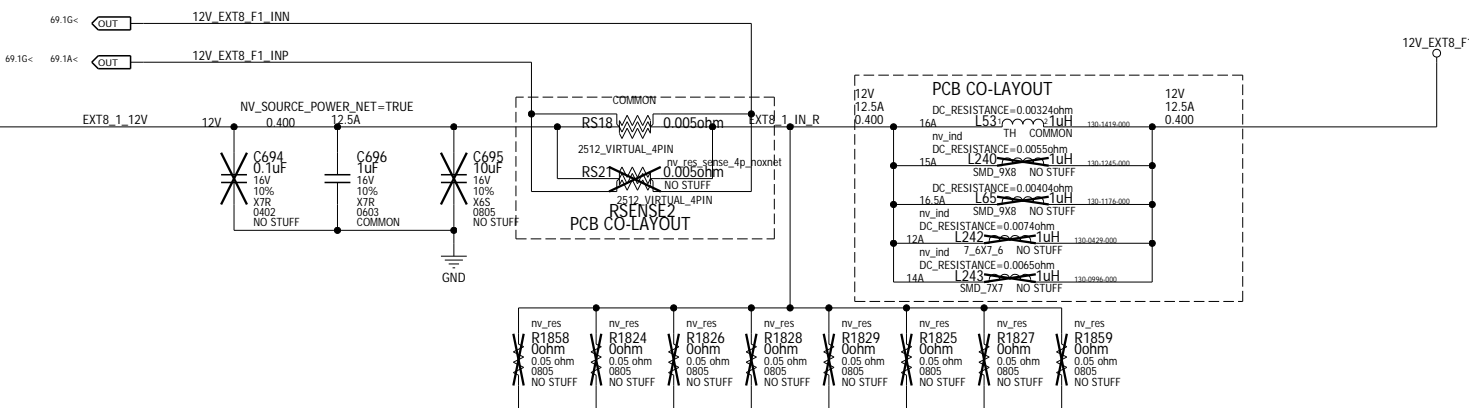
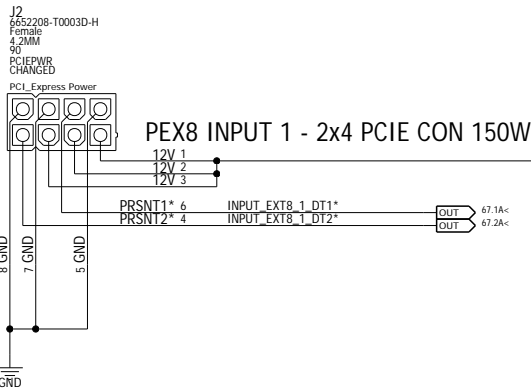
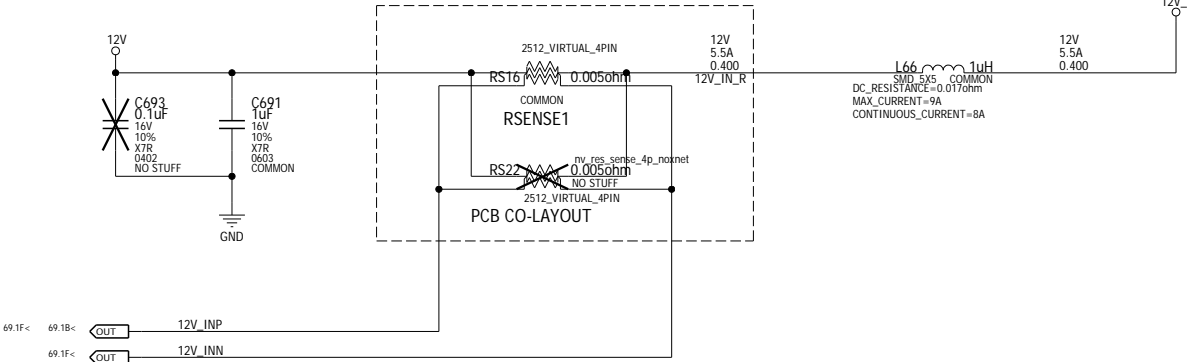
PS: Inputs, Filtering, and Monitoring



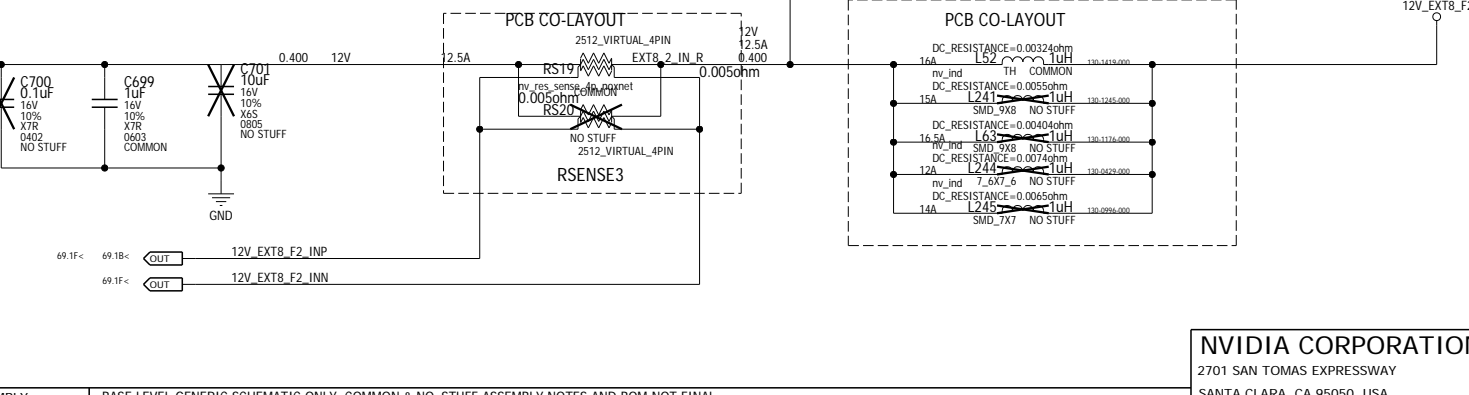
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



QD SKU CABLE



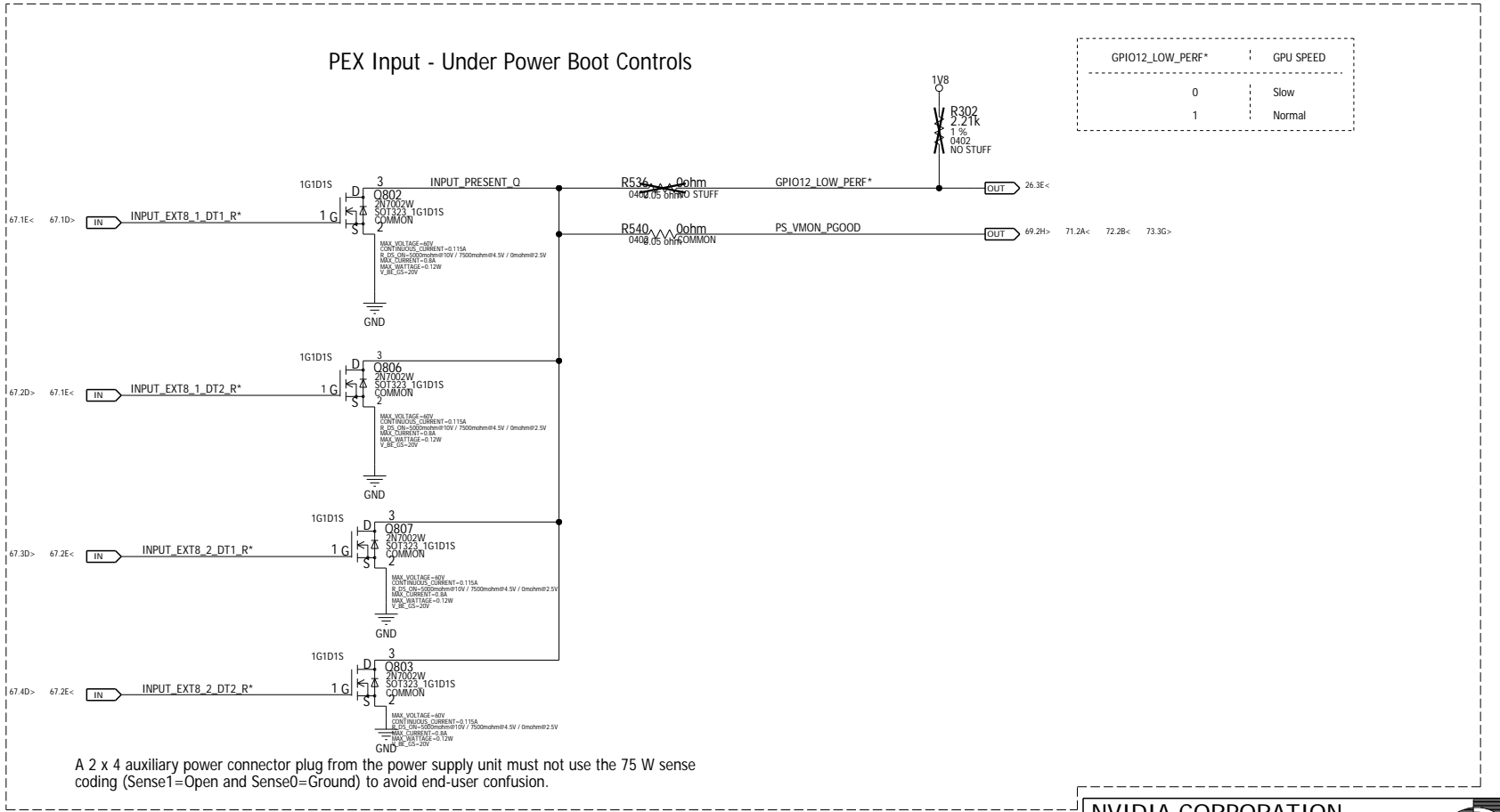
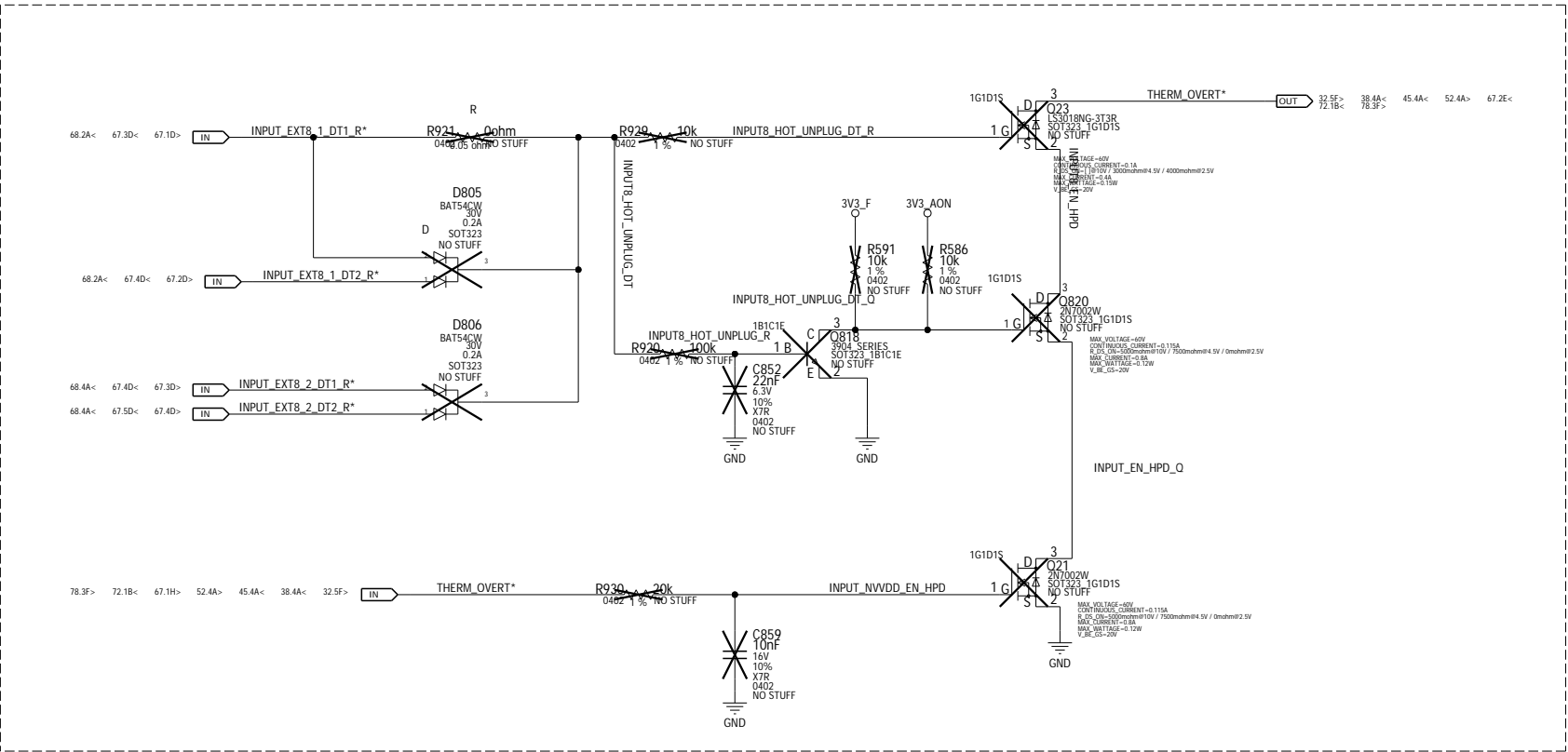
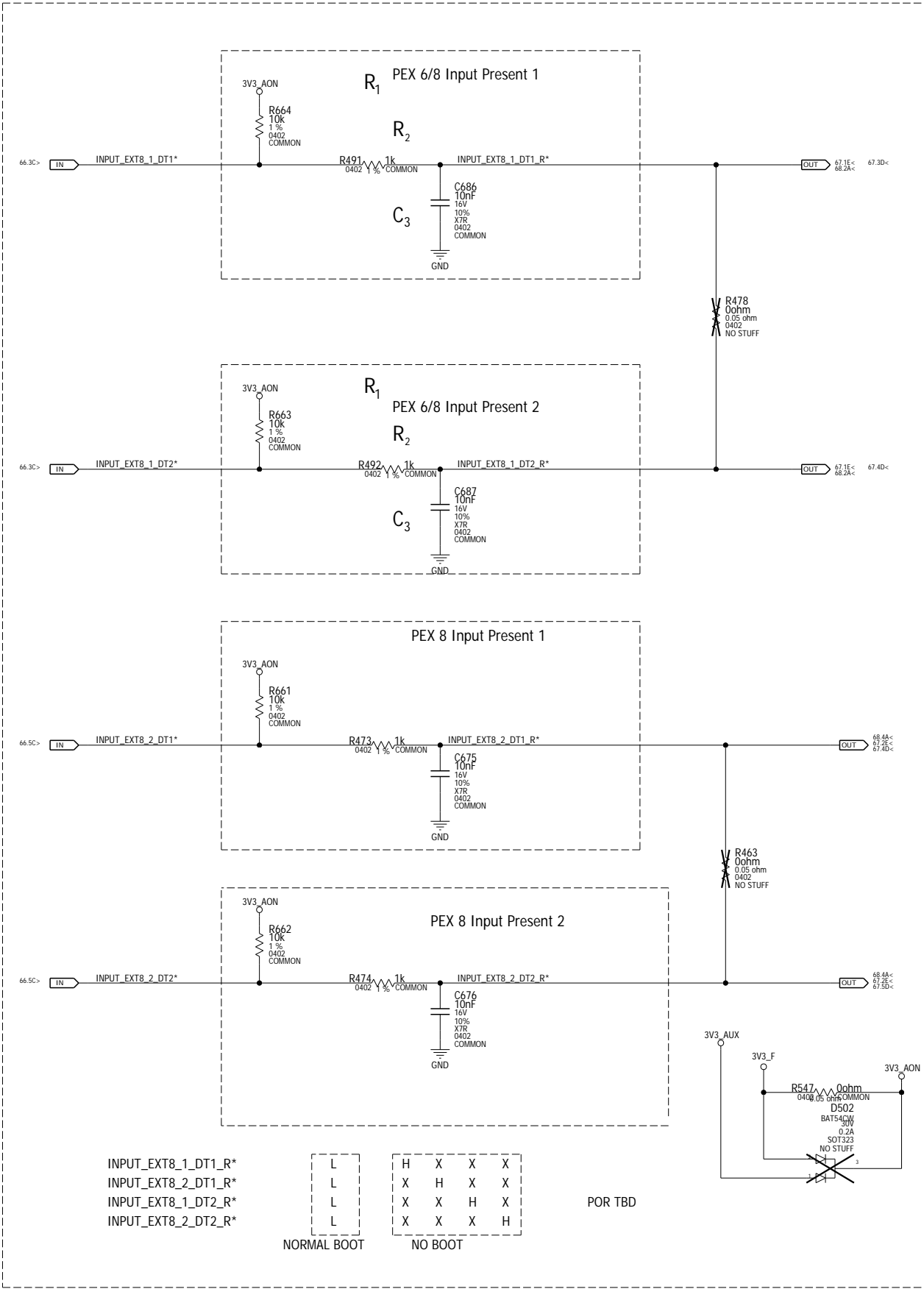
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PS: 12V Current Steering & Hot Unplug Detect



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: HOT UNPLUG

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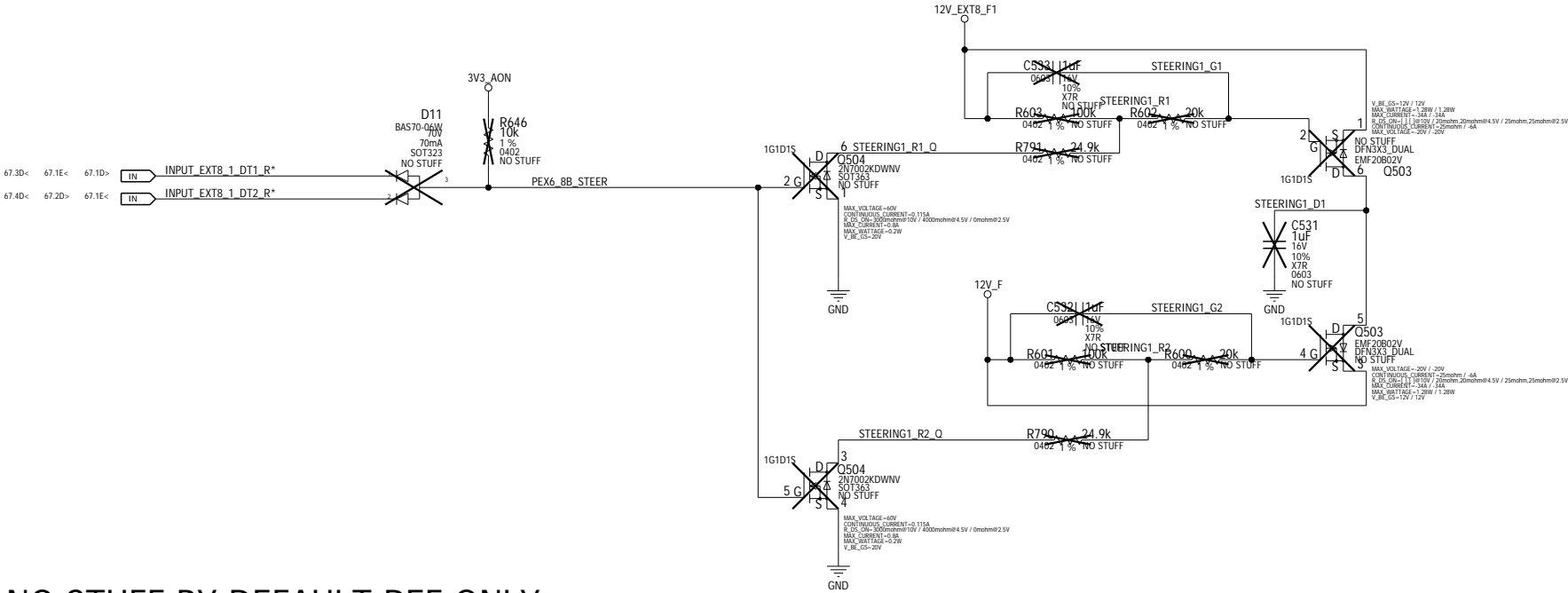


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DATE	15-JUN-2020

PS: Discrete Steering

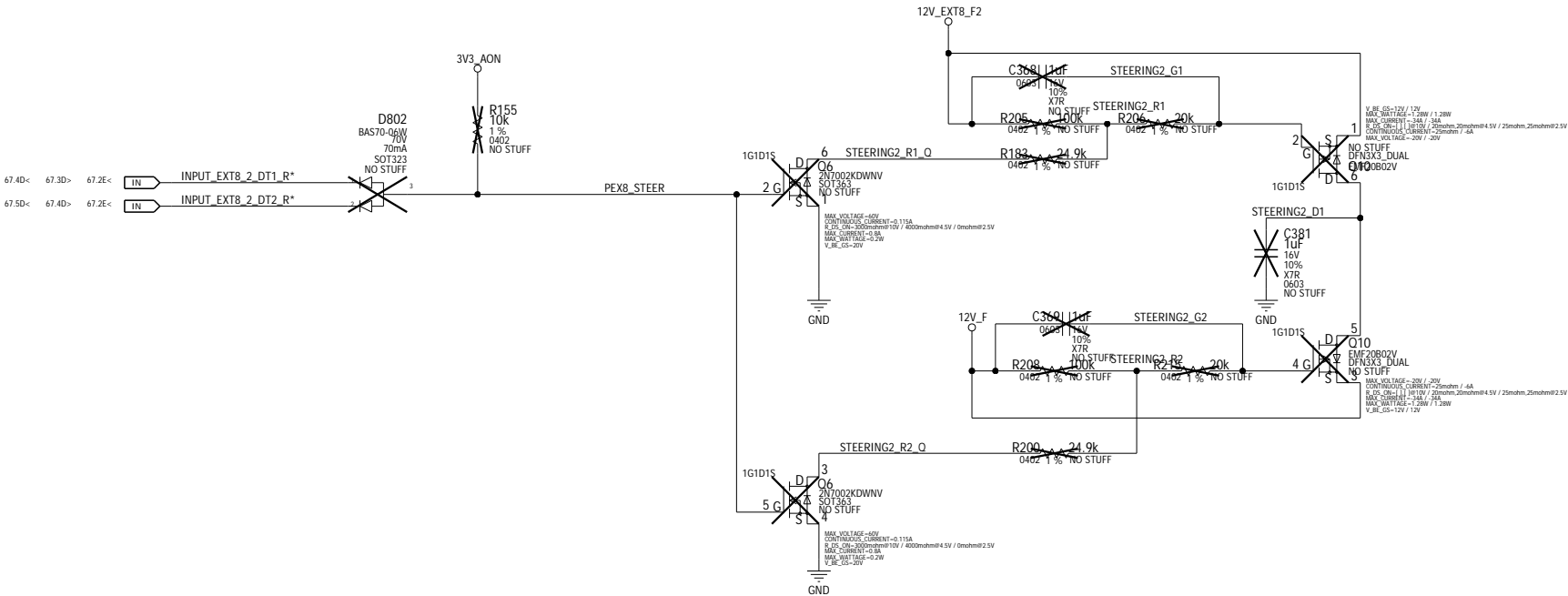
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2



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PCB REV PG132-A02

BOM REV C

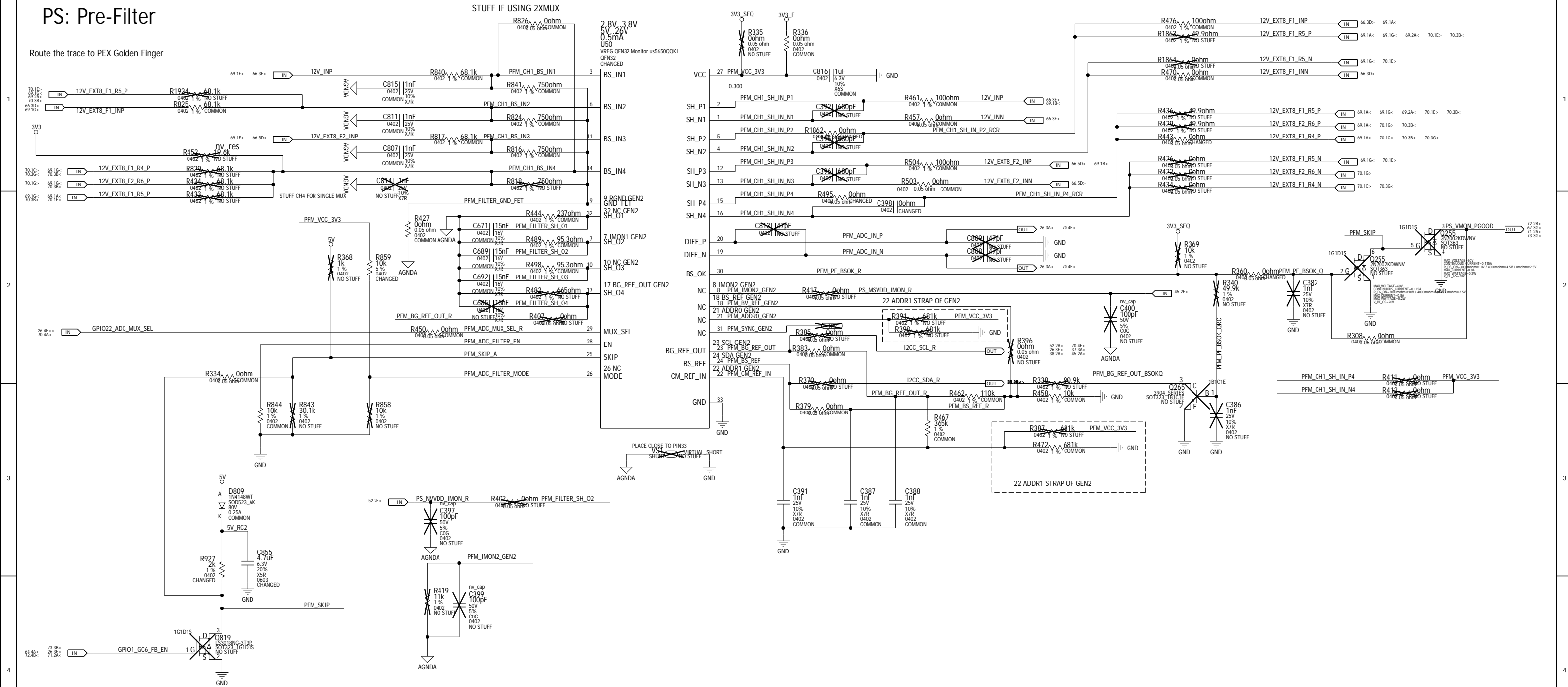
PAGE 68 OF 79

DATE 15-JUN-2020

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: Discrete Power Steering

PS: Pre-Filter

Route the trace to PEX Golden Finger



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: PREFILTER

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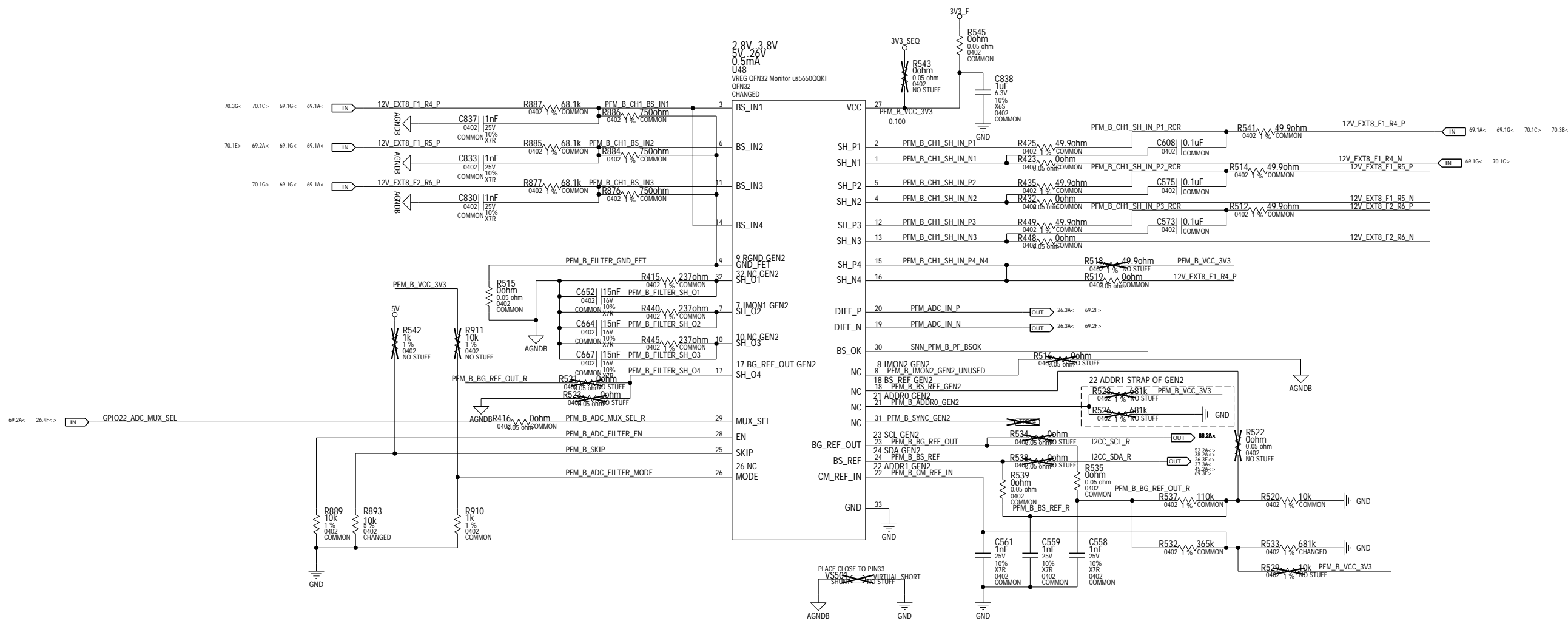
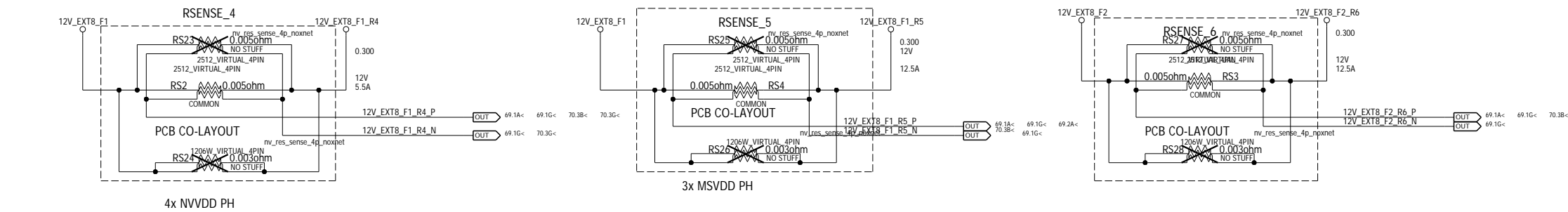
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PCB REV	PG132-A02	PAGE	69 OF 79
BOM REV	C	DATE	15-JUN-2020



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PS: Pre-Filter B



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: PREFILTER B

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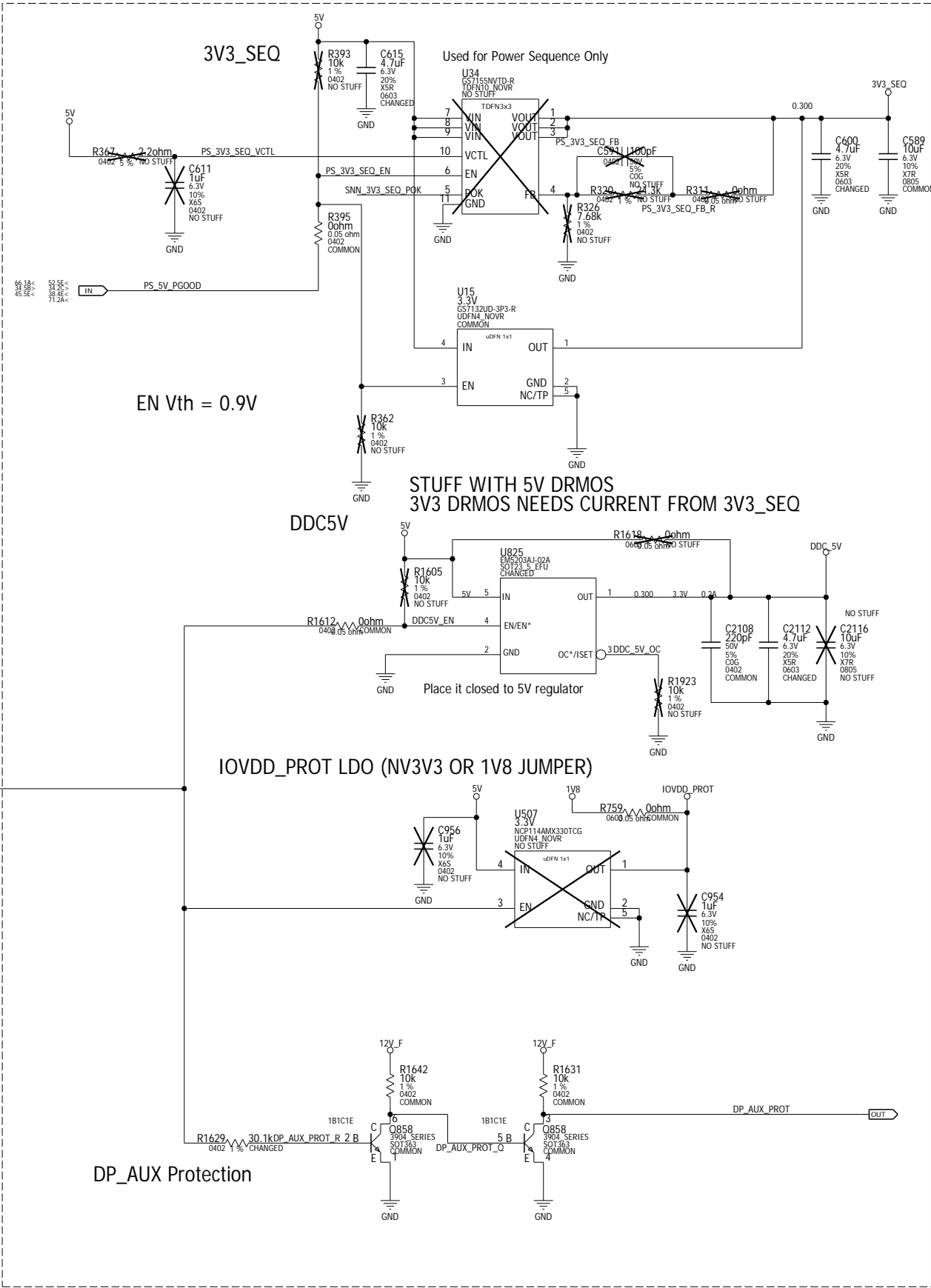
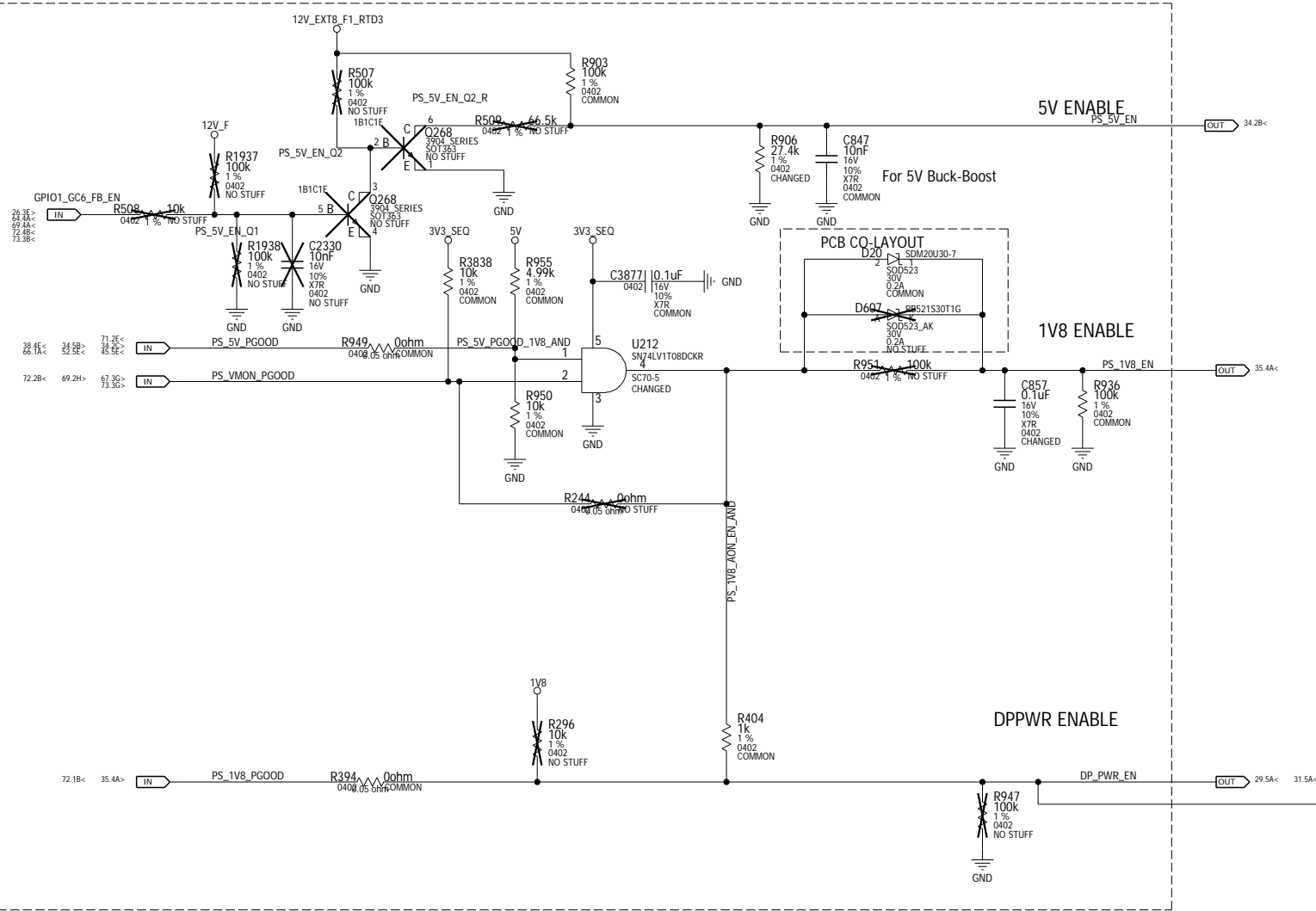
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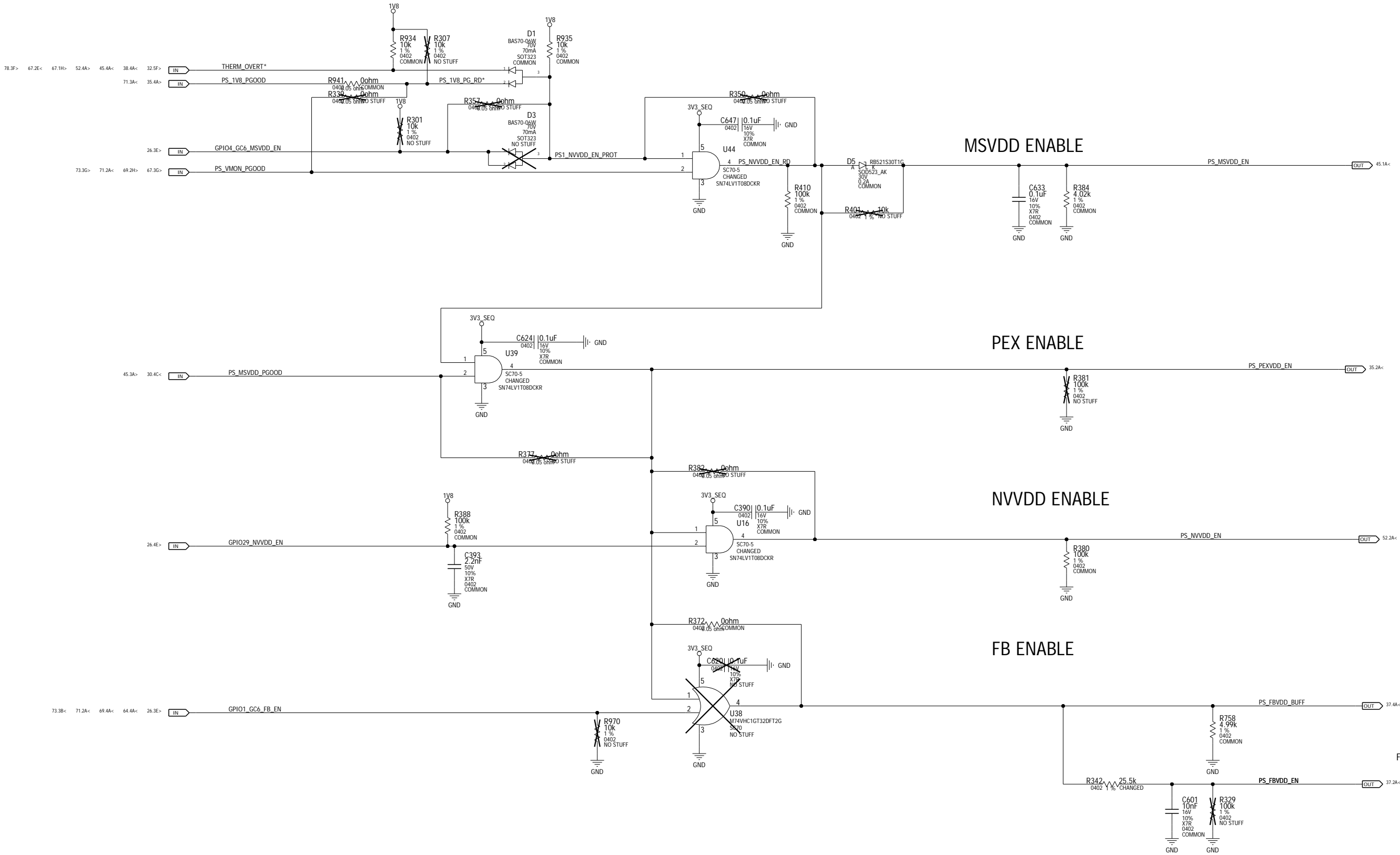
NV_PN	600-1G132-0030-300
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SEQUENCE:5V,1V8,3V3_SEQ ENABLE



SEQUENCE:NV,PEX,FB ENABLE



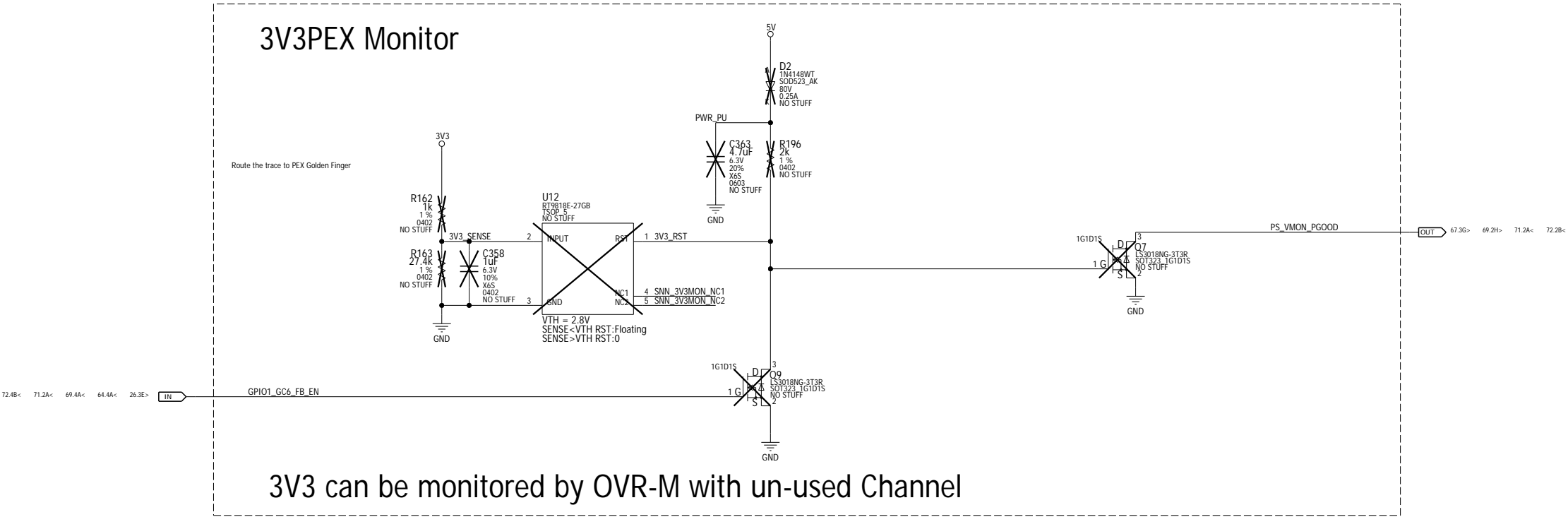
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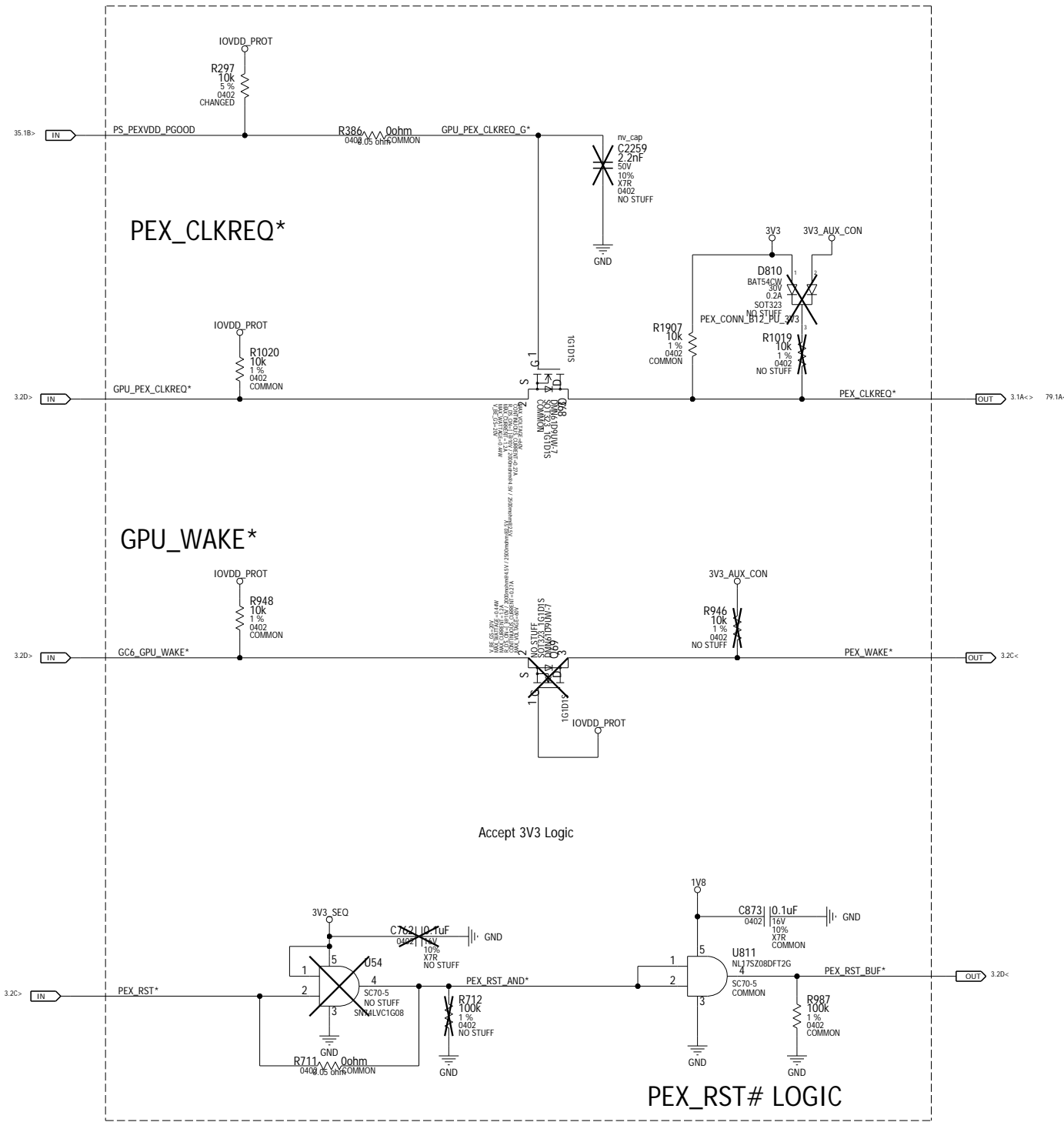


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Sequence: 3V3 MONITOR



SEQUENCE:MISC



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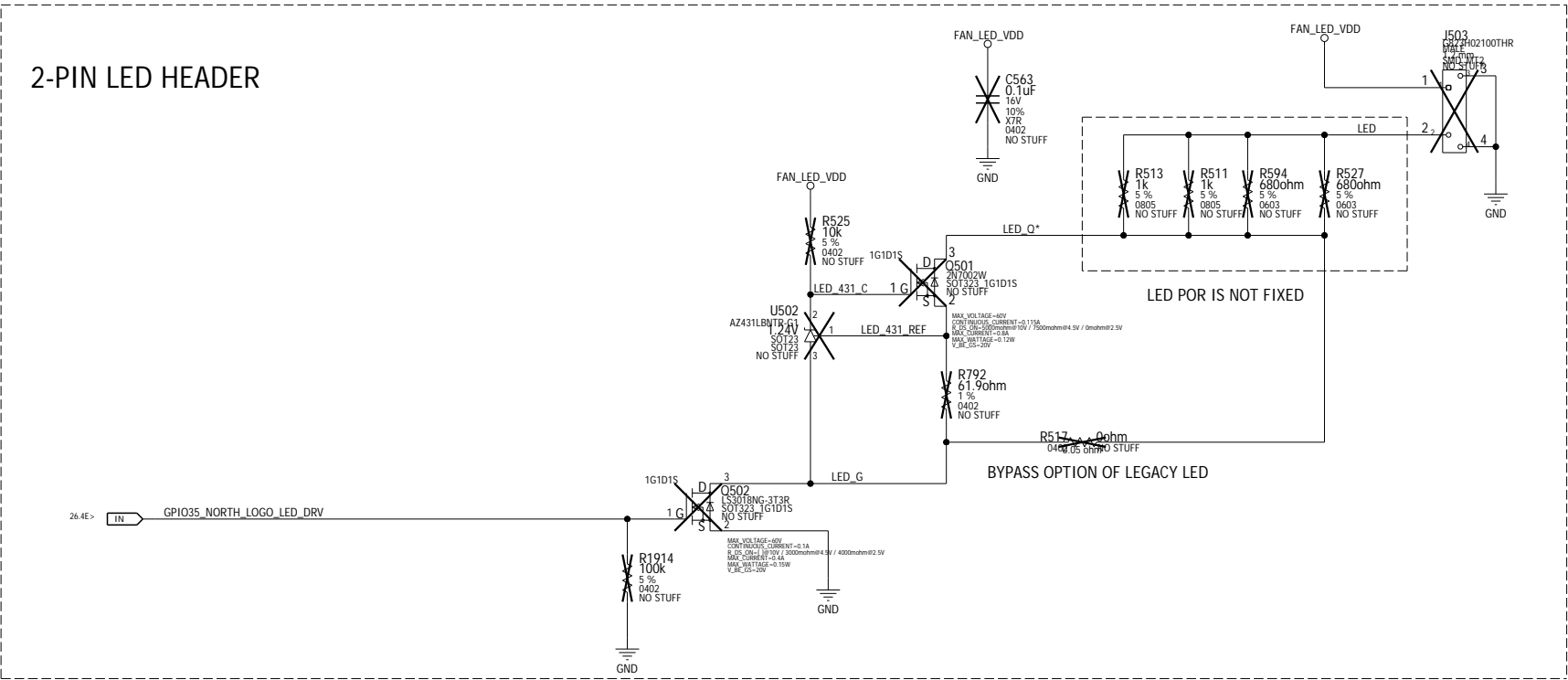


NV_PN	600-1G132-0030-300	PAGE	74 OF 79
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BOM REV	C		

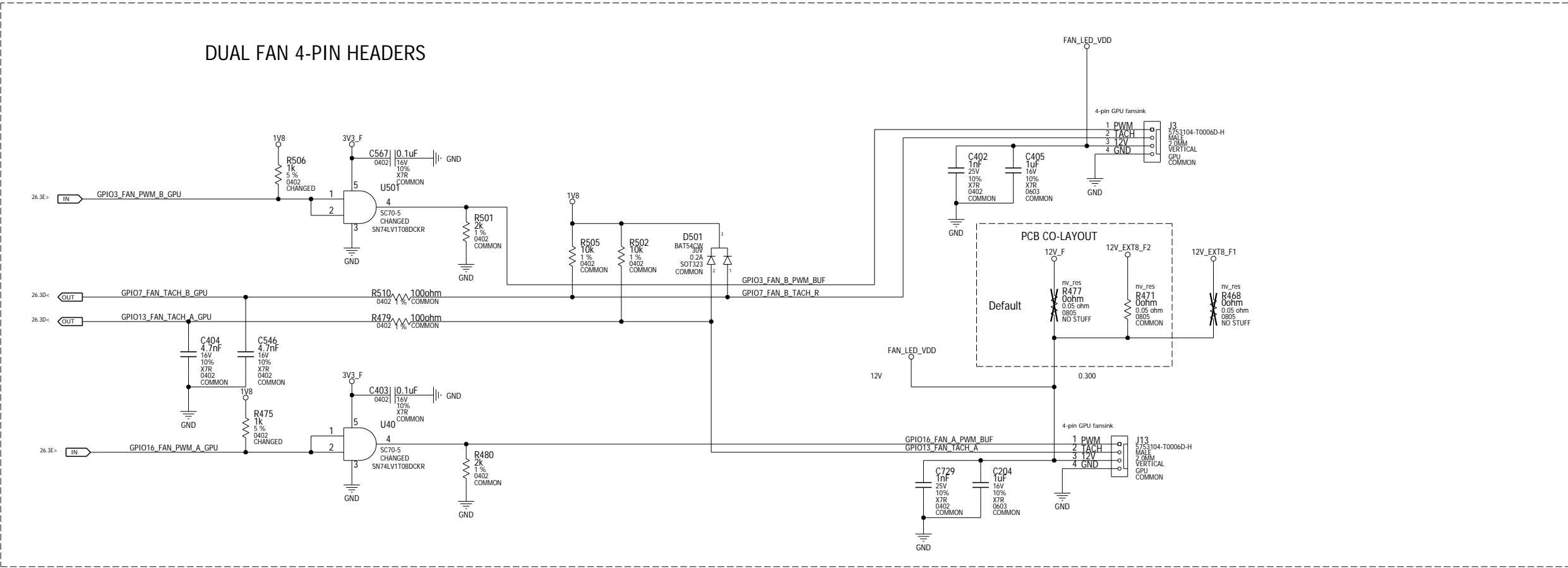
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Sequence: MISC

MISC: LED & FAN

2-PIN LED HEADER

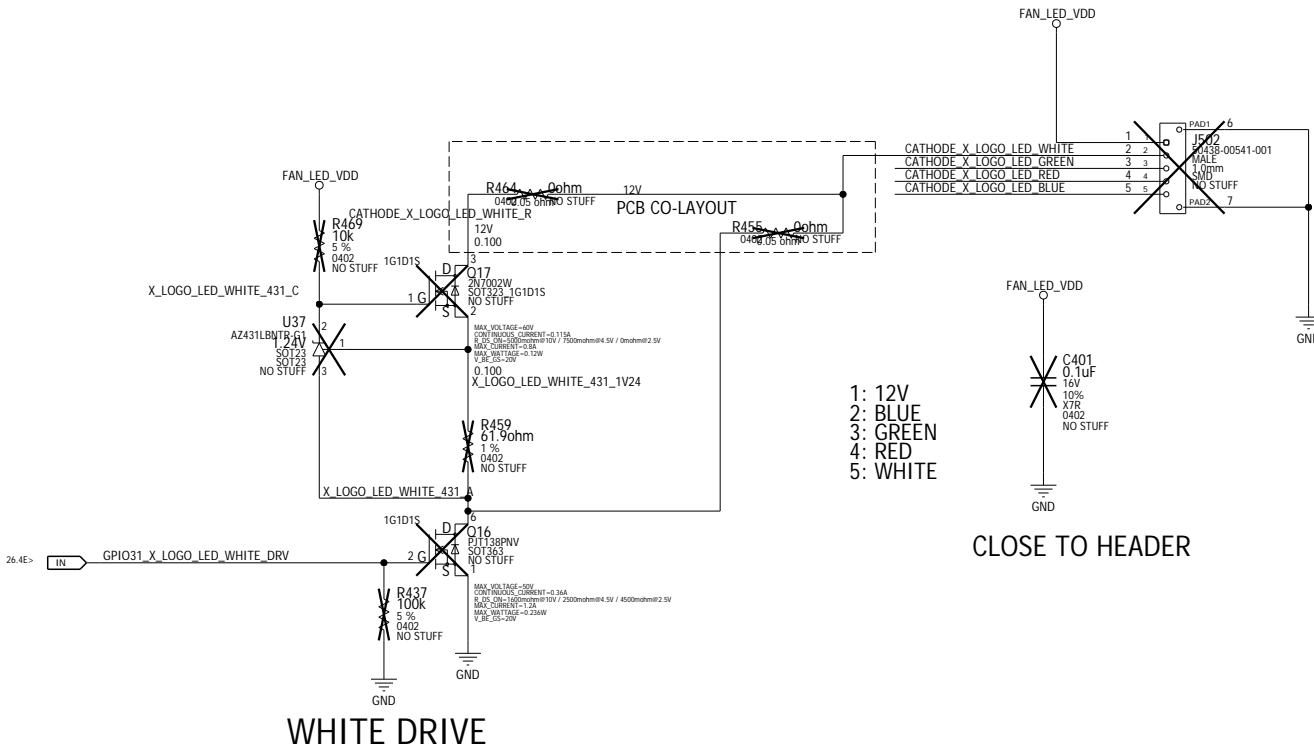


DUAL FAN 4-PIN HEADERS

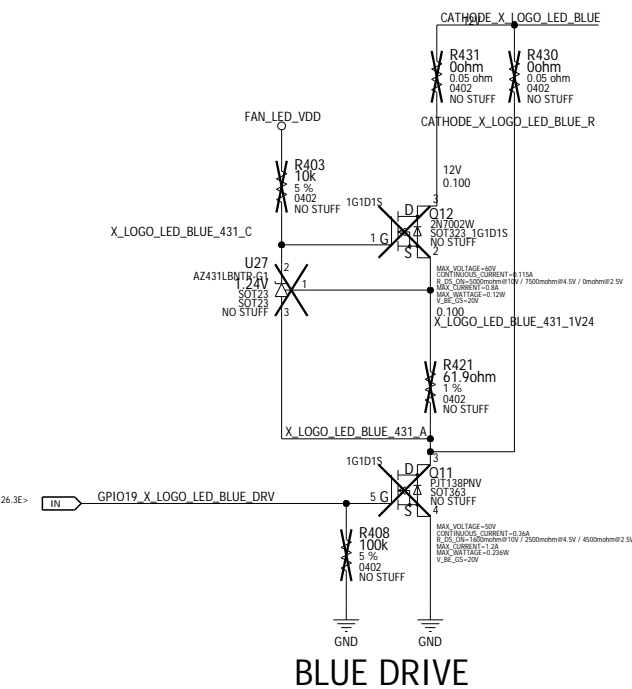
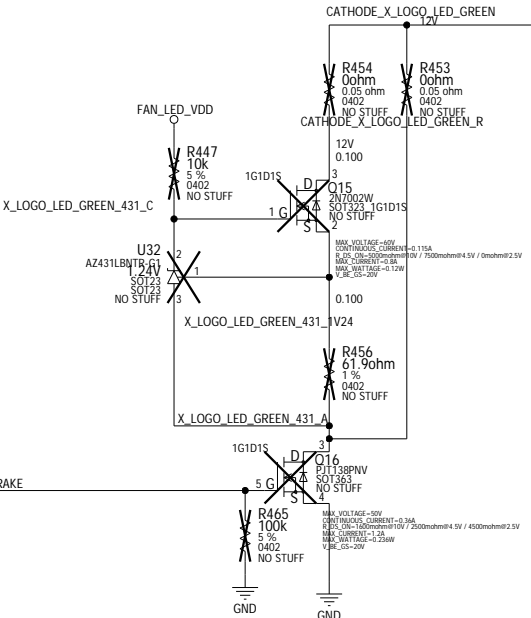
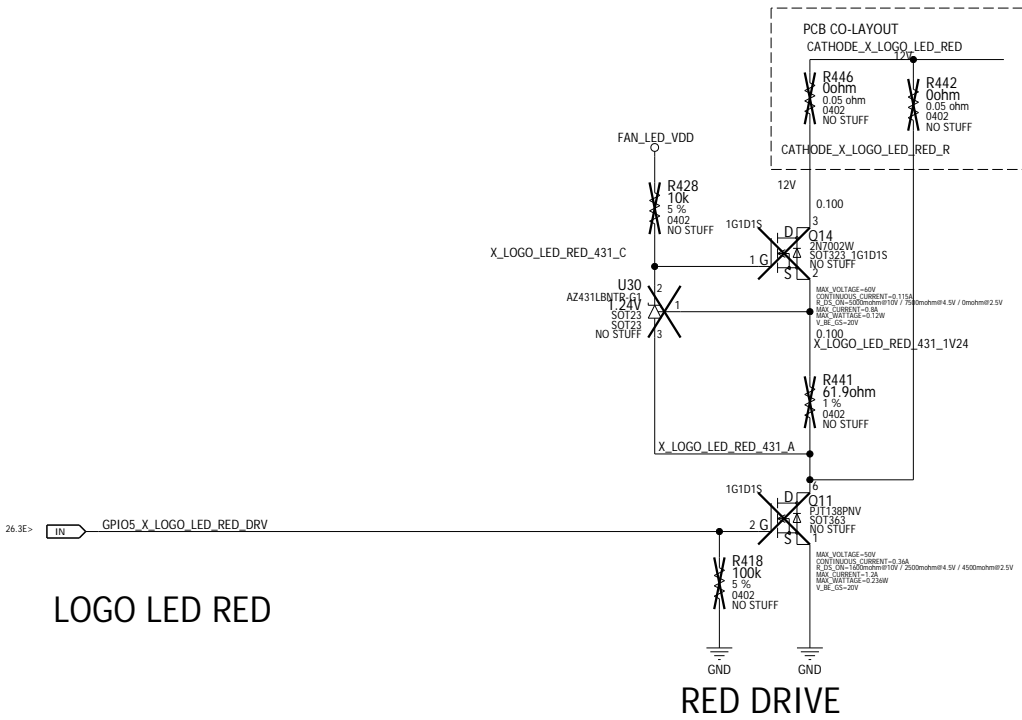


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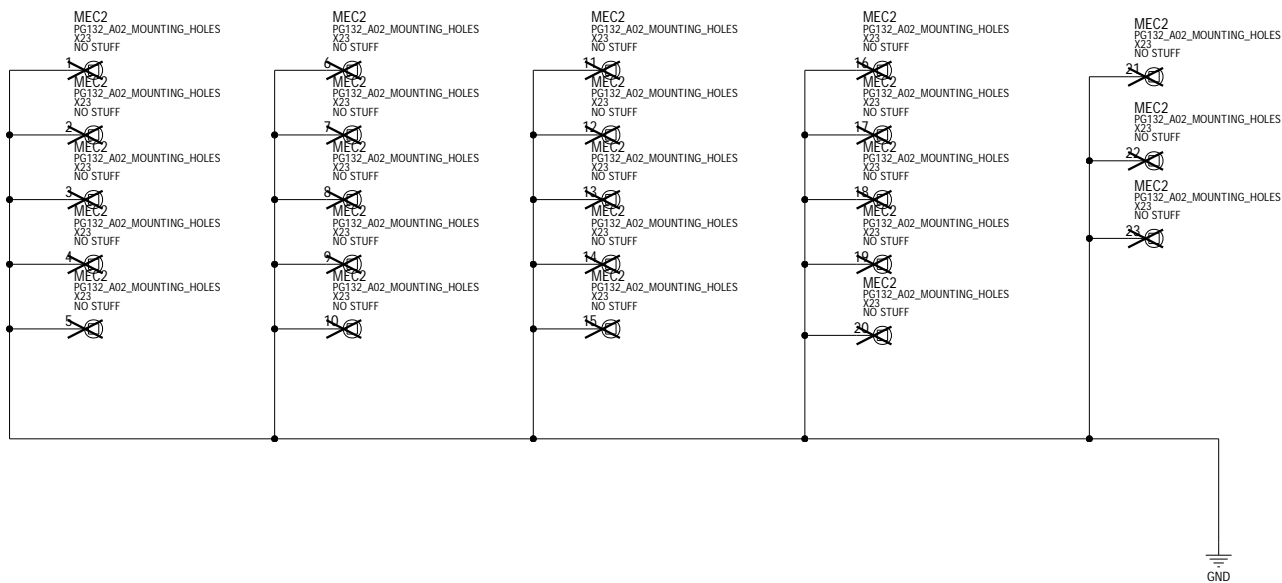
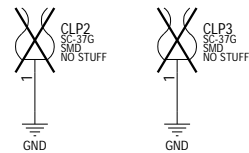
MISC: RGBW LED REF



CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALIGN WITH PASH
IF ADDITIONAL POWER CONSUPTION R
NEEDED, IT SHOULD BE ON LED MOD.



Mechanical: Mounting holes



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MECH

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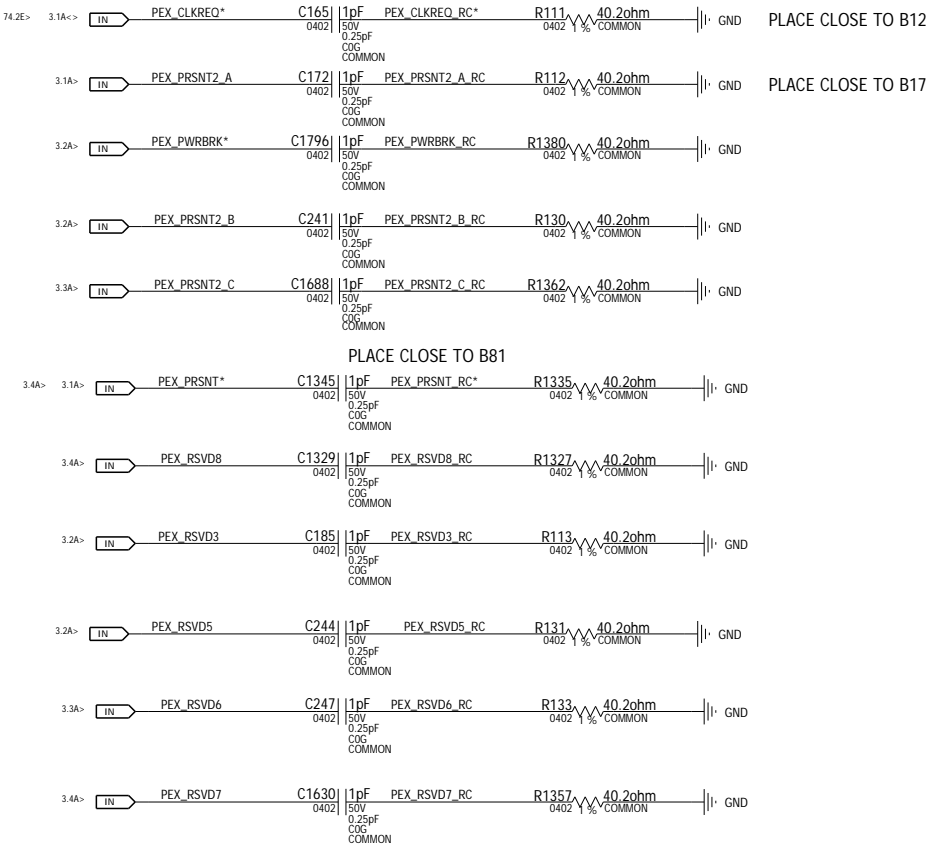
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PCI TERM



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